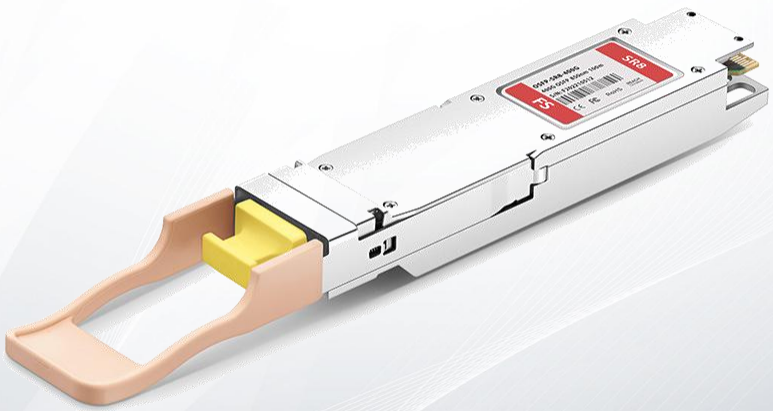
400GBASE-SR8 OSFP PAM4 850nm 100m MTP/MPO MMF Transceiver

OSFP-SR8-400G



Application

- Data Center Interconnect
- 400G Ethernet
- Infiniband Interconnects
- Enterprise Networking

Features

- Maximum Power Consumption 12W
- MPO-16 Connector
- Up to 100m Transmission on Multi-mode Fiber (MMF) OM3 with FEC
- Operating Case Temperature: 0 to 70℃
- 8 Parallel Lanes on 850nm Center Wavelength
- 8x53.125Gb/s Electrical Interface (400GAUI-8)
- Data Rate 53.125Gbps (PAM4) per Channel
- RoHS Compliant
- OSFP MSA Compliant
- Compliant to IEEE 802.3bs Specification

Description

The 400GBASE-SR8 OSFP transceiver supports up to 100m link lengths over multimode fiber (MMF) with MTP/MPO-16 connector. This transceiver is compliant with OSFP MSA, IEEE 802.3bs protocol and 400GAUI-8 standards. The 400 Gigabit Ethernet signal is carried over eight wavelengths. Multiplexing and demultiplexing of the eight wavelengths are managed within the device. It is suitable for 400G Ethernet, Data Center and Cloud Networks.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature Range	T_S	-40	85	℃
Operating Temperature	T_{OP}	0	70	℃
Power Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity(Non-Condensation)	RH	0	85	%

II. Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	T_{OP}	0		70	℃	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, Each Lane(PAM4)			26.5625		GBd	
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance with OM3	D	0.5		100	m	2

Notes:
1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

III. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Consumption				12	W	
Supply Current	I_{CC}			3.63	A	
Transmitter						
Signaling Rate, Each Lane	TP1	26.5625 ± 100ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE802.3-2015Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE802.3-2015Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range(Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Receiver						
Signaling Rate, Each Lane	TP4	26.5625 ± 100ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE802.3-2015Equation(83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE802.3-2015Equation(83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width(ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width(ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage(Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

IV. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λ_C	840	850	860	nm	
Data Rate, Each Lane			26.5625±100ppm		GBd	
Modulation Format			PAM4			
RMS Spectral Width(Modulated)	Δλrms			0.6	nm	
Average Launch Power, Each Lane	PAVG	-6.5		4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), Each Lane	POMA	-4.5		3	dBm	2
Launch Power in OMA_{outer} Minus TDECQ, Each Lane		-5.9			dB	
Transmitter and Dispersion Eye Clouser for PAM4, Each Lane	TDECQ			4.5	dB	
Extinction Ratio	ER	3			dB	
Optical Return Loss Tolerance	TOL			12	dB	
Average Launch Power of OFF Transmitter, Each Lane	Poff			-30	dBm	
Encircled Flux			≥86%at19μm≤30%at4.5μm			

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Receiver						
Center Wavelength	λ_C	840	850	860	nm	
Data Rate, Each Lane			26.5625 ± 100ppm		GBd	
Modulation Format			PAM4			
Damage Threshold, Each Lane	TH_d	5			dBm	3
Average Receive Power, Each Lane		-7.9		4	dBm	4
Receive Power(OMA_{outer}), Each Lane				3	dBm	
Receiver Sensitivity(OMA_{outer}), Each Lane	SEN			-6.5	dBm	5
Stressed Receiver Sensitivity(OMA_{outer}), Each Lane	SRS			-3	dBm	6
Receiver Reflectance	R_R			-12	dB	
LOS Assert	LOS_A	-30			dBm	
LOS De-assert	LOS_D			-12	dBm	
LOS Hysteresis	LOS_H	0.5			dB	

Notes:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1 dB , the OMAouter (min) must exceed the minimum value specified here.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver Sensitivity OMAouter, each lane (max) is informative and is defined for a BER of 2.4x10-4.
6. Measured with conformance test signal at receiver input for the BER of 2.4x10-4.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

V. Digital Diagnostic Monitor Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Temperature Monitor Absolute Error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

VI. Pin Configuration

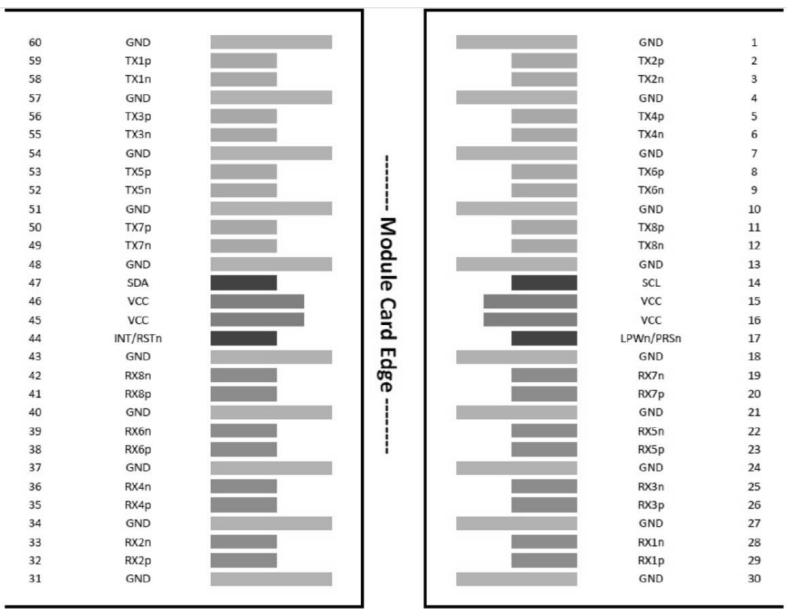


Figure 1: Pin out of Connector Block on Host Board

VII. Transceiver Pin Descriptions

Pin No.	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial Interface Clock	LVCMOS-I/O	Bi-directional	3
15	V_{CC}	+3.3V Power		Power from Host	2
16	V_{CC}	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3

Pin No.	Symbol	Description	Logic	Direction	Plug Sequence
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1

Pin No.	Symbol	Description	Logic	Direction	Plug Sequence
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3
45	V_{CC}	+3.3V Power		Power from Host	2
46	V_{CC}	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial Interface Data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

VIII. Block Diagram of Transceiver

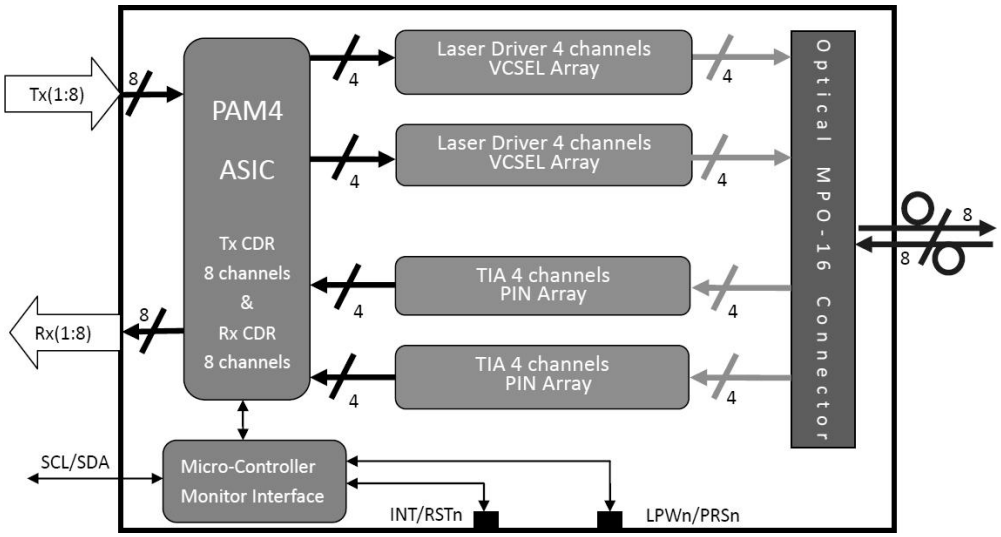


Figure 2

IX. Mechanical Dimensions

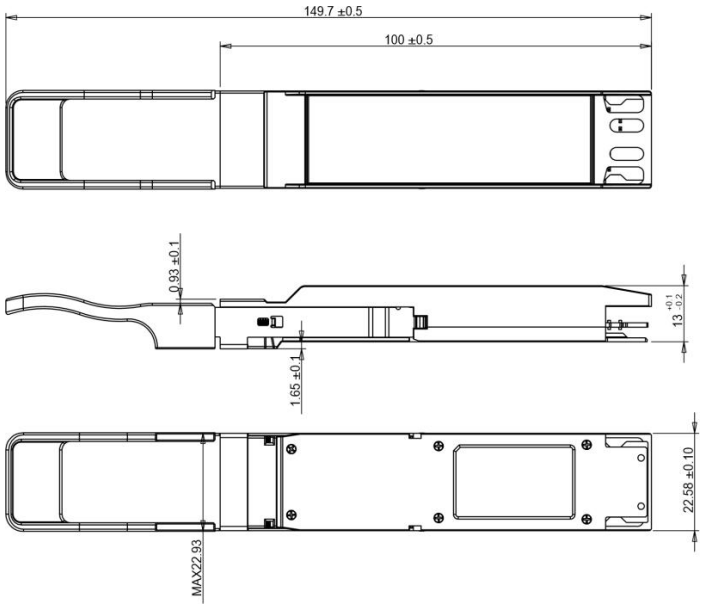


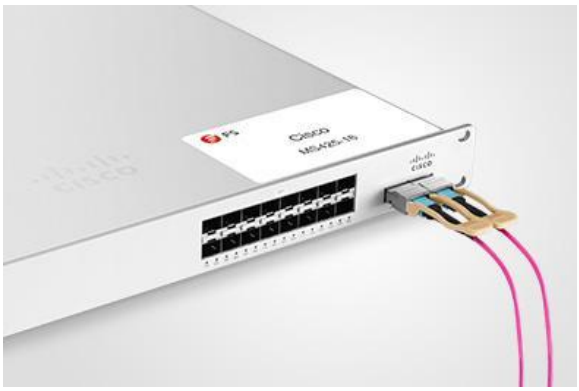
Figure 3

Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.

Cisco Catalyst C9500-24Y4C



Cisco MS425-16

Brocade VDX 6940-144S

Dell EMC Networking Z9100-ON

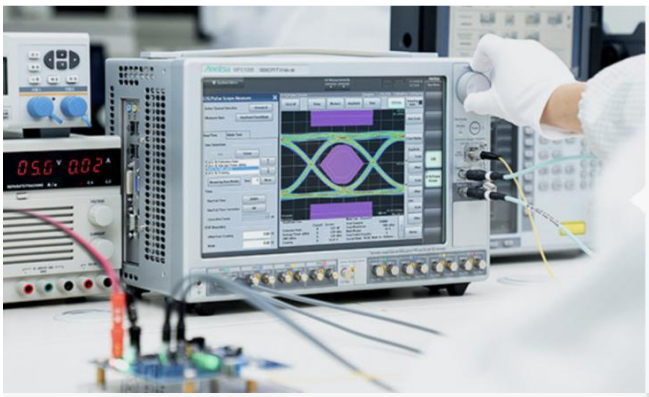
Force⑩tm S60-44T

HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Signal Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator to ensure the input and output signal quality.

- Eye Pattern Measurements: Jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic changes in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0 °C to 70 °C
- Extended: -5 °C to 85 °C
- Industrial: -40 °C to 85 °C

3. Transfer Rate and Protocol Testing

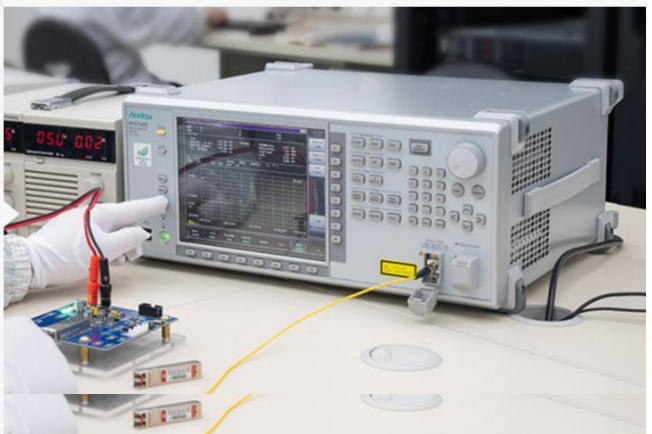
Test the actual transfer data rate and the transmission ability under different protocols with Network Master Pro.

- Ethernet
- Fibre Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

Part Number	Description
QSFPDD-SR8-400G	QSFP-DD 400GBASE-SR8 850nm 100m Transceiver
OSFP-SR8-400G	OSFP 400GBASE-SR8 850nm 100m Transceiver
QDD-DR4-400G-Si	QSFP-DD 400GBASE-DR4 1310nm 500m Silicon Photonics Transceiver
QSFPDD-XDR4-400G	QSFP-DD 400GBASE-DR4+ 1310nm 2km Transceiver
QSFPDD-FR4-400G	QSFP-DD 400GBASE-FR4 1310nm 2km Transceiver
QSFPDD-LR4-400G	QSFP-DD 400GBASE-LR4 1310nm 10km Transceiver
QSFPDD-LR8-400G	QSFP-DD 400GBASE-LR8 1310nm 10km Transceiver
QSFPDD-PLR4-400G	QSFP-DD 400GBASE-PLR4 1310nm 10km Transceiver
QSFPDD-ER8-400G	QSFP-DD 400GBASE-ER8 QSFP-DD PAM4 1310nm 40km Transceiver

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