FS

400G QSFP-DD To 2 QSFP56 Passive Copper Breakout Direct Attach Cable (PCC)

Application

- Data Center & Networking Equipment
- Servers / Storage Devices
- High Performance Computing (HPC)
- Switches / Routers

Standards Compliance

- IEEE802.3Bj, By, IEEE802.3CD
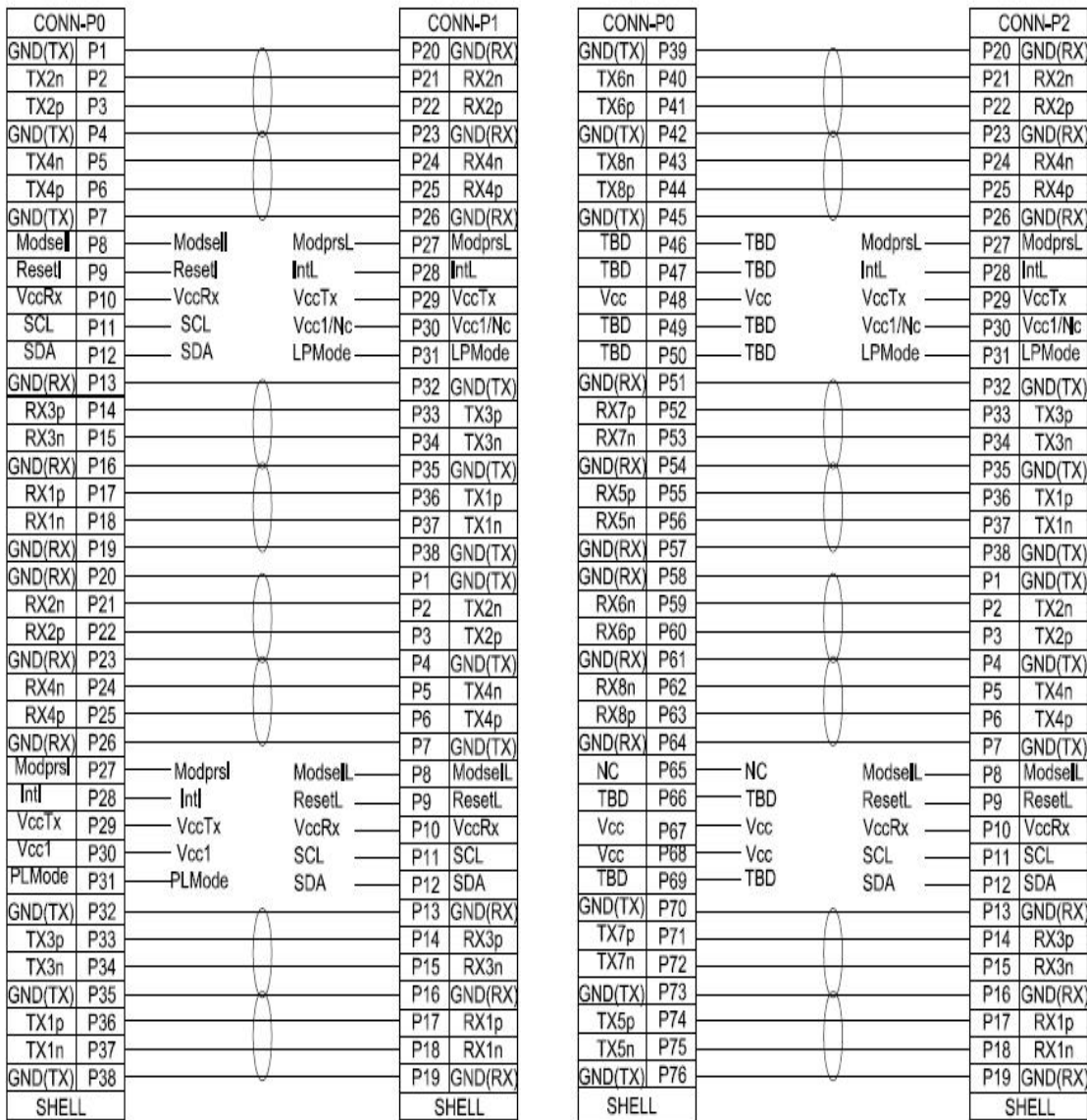- RoHS Compliant

Features

- Compliant with QSFP-DD MSA Specification Rev 3.4
- SFF-8679 electrical interface compliant
- SFF-8636 management interface support
- Support 50G (PAM4) electrical data rates / channel
- I²C for EEPROM communication, pull to Release latch design
- Excellent EMI/EMC performance 360 degree cable shield termination
- Advantage dual side pre-solder automated assembly technologies
- Low loss, stronger mechanical features, more flexible
- QSFP-DD modules will be backwards compatible, allowing them to support existing QSFP modules and provide flexibility for end users and system designers

Description

In an effort to keep up with the demands of higher performance and increasing amounts of memory bus bandwidth, FS designers are working to revise, extend and update the solution. FS 400G QSFP-DD passive cable assembly can provide new generation performance of QSFP by higher date transfer rate. At the same time, FS QSFP-DD TO 2 QSFP56 cable choose dual side drain cable and self-designed PCBA, provide low loss, less skew and better NEXT. 360 degree EMI crimping shielding and Zinc Die-cast shell designing make the product high-performance. And all the designing is based on the industry standard specifications, such as SFF-8679, SFF-8636 and QSFP-DD TO 2 QSFP56 MSA specification rev 4.0.

I. Schematic

WIRING TABLE—-QSFP-DD TO 2QSFP

CONN-P0		P0 mid	P1 mid		CONN-P1
GND(TX)	P1			P20	GND(RX)
TX2n	P2			P21	RX2n
TX2p	P3			P22	RX2p
GND(TX)	P4			P23	GND(RX)
TX4n	P5			P24	RX4n
TX4p	P6			P25	RX4p
GND(TX)	P7			P26	GND(RX)
Modsel	P8	Modsel	ModprsL	P27	ModprsL
Resetl	P9	Resetl	IntL	P28	IntL
VccRx	P10	VccRx	VccTx	P29	VccTx
SCL	P11	SCL	Vcc1/Nc	P30	Vcc1/Nc
SDA	P12	SDA	LPMode	P31	LPMode
GND(RX)	P13			P32	GND(TX)
RX3p	P14			P33	TX3p
RX3n	P15			P34	TX3n
GND(RX)	P16			P35	GND(TX)
RX1p	P17			P36	TX1p
RX1n	P18			P37	TX1n
GND(RX)	P19			P38	GND(TX)
GND(RX)	P20			P1	GND(TX)
RX2n	P21			P2	TX2n
RX2p	P22			P3	TX2p
GND(RX)	P23			P4	GND(TX)
RX4n	P24			P5	TX4n
RX4p	P25			P6	TX4p
GND(RX)	P26			P7	GND(TX)
Modprsl	P27	Modprsl	ModselL	P8	ModselL
Intl	P28	Intl	ResetL	P9	ResetL
VccTx	P29	VccTx	VccRx	P10	VccRx
Vcc1	P30	Vcc1	SCL	P11	SCL
PLMode	P31	PLMode	SDA	P12	SDA
GND(TX)	P32			P13	GND(RX)
TX3p	P33			P14	RX3p
TX3n	P34			P15	RX3n
GND(TX)	P35			P16	GND(RX)
TX1p	P36			P17	RX1p
TX1n	P37			P18	RX1n
GND(TX)	P38			P19	GND(RX)
SHELL					SHELL

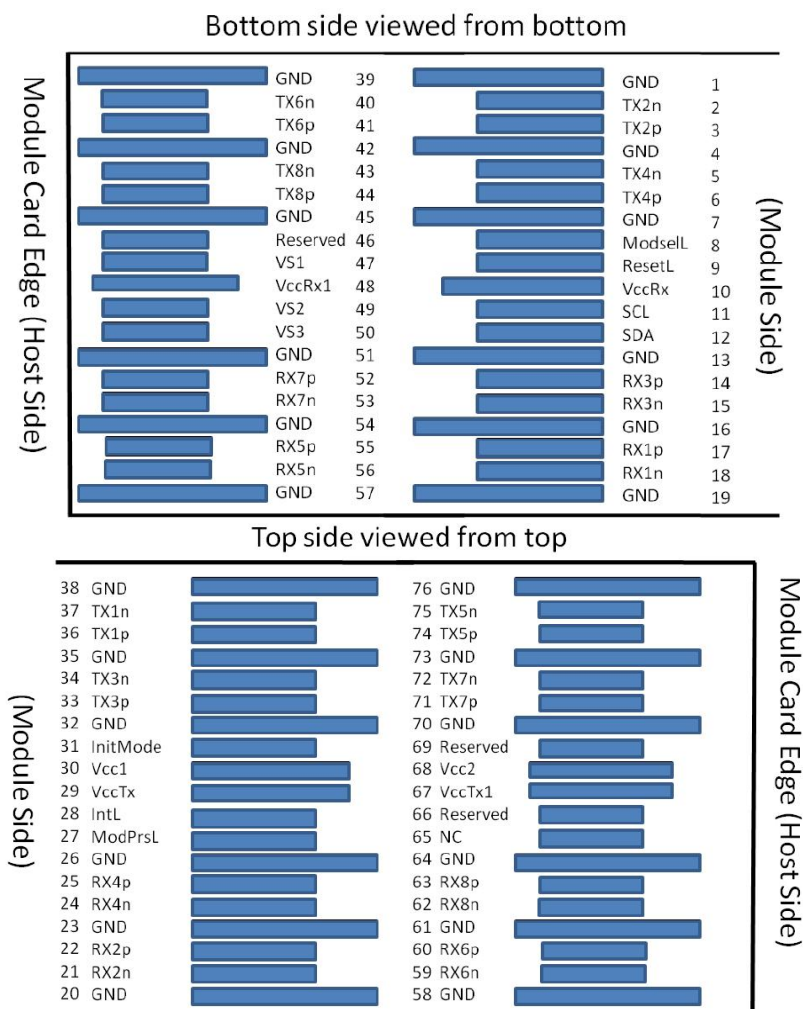| CONN-P0		P0 mid	P2 mid		CONN-P2
GND(TX)	P39			P20	GND(RX)
TX6n	P40			P21	RX2n
TX6p	P41			P22	RX2p
GND(TX)	P42			P23	GND(RX)
TX8n	P43			P24	RX4n
TX8p	P44			P25	RX4p
GND(TX)	P45			P26	GND(RX)
TBD	P46	TBD	ModprsL	P27	ModprsL
TBD	P47	TBD	IntL	P28	IntL
Vcc	P48	Vcc	VccTx	P29	VccTx
TBD	P49	TBD	Vcc1/Nc	P30	Vcc1/Nc
TBD	P50	TBD	LPMode	P31	LPMode
GND(RX)	P51			P32	GND(TX)
RX7p	P52			P33	TX3p
RX7n	P53			P34	TX3n
GND(RX)	P54			P35	GND(TX)
RX5p	P55			P36	TX1p
RX5n	P56			P37	TX1n
GND(RX)	P57			P38	GND(TX)
GND(RX)	P58			P1	GND(TX)
RX6n	P59			P2	TX2n
RX6p	P60			P3	TX2p
GND(RX)	P61			P4	GND(TX)
RX8n	P62			P5	TX4n
RX8p	P63			P6	TX4p
GND(RX)	P64			P7	GND(TX)
NC	P65	NC	ModselL	P8	ModselL
TBD	P66	TBD	ResetL	P9	ResetL
Vcc	P67	Vcc	VccRx	P10	VccRx
Vcc	P68	Vcc	SCL	P11	SCL
TBD	P69	TBD	SDA	P12	SDA
GND(TX)	P70			P13	GND(RX)
TX7p	P71			P14	RX3p
TX7n	P72			P15	RX3n
GND(TX)	P73			P16	GND(RX)
TX5p	P74			P17	RX1p
TX5n	P75			P18	RX1n
GND(TX)	P76			P19	GND(RX)
SHELL					SHELL

II. Mechanical Structure Characteristics Of PlugI

1. Raw Cable -- Support 28~30AWG, 100ohm, Silver plated, vw-1, RoHS2.0.

2. PCB –High Speed Very low loss material M6,8 Layers Design; Gold finger plated gold 30u" min., nickel plated 150~700u"; pad: immersion gold 1u" min., nickel plated 100u"min. 94v-0, RoHS2.0;

3. Upper shell -- Zinc Die-cast, with Cu plated 280u" min. overall and Ni plated 120u" min.

4. Bottom shell -- Zinc Die-cast, with Cu plated 280u" min. overall and Ni plated 120u" min.

5. Latch-- Stainless steel ,SUS304 + PA66 CM3004,black;

6. Spring -- Stainless steel ,SUS301EH;

7. Rivet -- Stainless Steel, SUS304;

8. SR (Strain Relief) -- PVC, 45P, BLACK, RoHS2.0.

9. Dust Cover—PVC, 60P, Blue, ANTI-STATIC, RoHS2.0.

III. Electrical Design

The electrical design of the QSFP-DD TO 2 QSFP cable assembly is fully compliant to QSFP-DD TO 2 QSFP Hardware Rev4.0 specifications. The electrical design included: a low loss design printed circuit board, DC block capacitances in the Rx channel, and EEprom chips for the management. Pin layout and function definition are shown in Figure and Table .

Bottom side viewed from bottom

Module Card Edge (Host Side):

Signal	Pin		Signal	Pin
GND	39		GND	1
TX6n	40		TX2n	2
TX6p	41		TX2p	3
GND	42		GND	4
TX8n	43		TX4n	5
TX8p	44		TX4p	6
GND	45		GND	7
Reserved	46		ModselL	8
VS1	47		ResetL	9
VccRx1	48		VccRx	10
VS2	49		SCL	11
VS3	50		SDA	12
GND	51		GND	13
RX7p	52		RX3p	14
RX7n	53		RX3n	15
GND	54		GND	16
RX5p	55		RX1p	17
RX5n	56		RX1n	18
GND	57		GND	19

(Module Side)

Top side viewed from top

(Module Side) / Module Card Edge (Host Side):

Pin	Signal		Pin	Signal
38	GND		76	GND
37	TX1n		75	TX5n
36	TX1p		74	TX5p
35	GND		73	GND
34	TX3n		72	TX7n
33	TX3p		71	TX7p
32	GND		70	GND
31	InitMode		69	Reserved
30	Vcc1		68	Vcc2
29	VccTx		67	VccTx1
28	IntL		66	Reserved
27	ModPrsL		65	NC
26	GND		64	GND
25	RX4p		63	RX8p
24	RX4n		62	RX8n
23	GND		61	GND
22	RX2p		60	RX6p
21	RX2n		59	RX6n
20	GND		58	GND

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	

15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2

30		Vccl	+3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	

45		GND	Ground	1
46		Reserved	For future use	3
47		VSI	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	

60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	

75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1. QSFP-DD TO 2 QSFP56 uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD TO 2 QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD TO 2 QSFP pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

IV. 2-Wires EEPROM Interface

The QSFP-DD TO 2 QSFP56 passive cable EEPROM is compliant with CMIS3.0 specification. Each connector contains a 256 bytes EEPROM at device address A0(h). The information for addresses 0 to 255 is listed below, see table 3. This information can be tailored to any customer request. Any address can be altered to display customer specific information.

A0h address	Name	Value	Description
0	Identifier	18	Type of Serial Module -- See SFF-8024,19h:OSFP 8X Pluggable Transceiver
1	Version ID	30	the upper nibble is the whole number part and the lower nibble is the decimal part.Example: 21h indicates version 2.1.

	Flat_mem		Upper memory flat or paged.0b=Paged memory 1b=Flat memory (only page 00h implemented)
	CLEI present		CLEI code present in upper page 00h
2	Reserved	80	Reserved
	TWI Maximum speed		Indicates maximum two-wire serial speed supported by module 00b=Module supports up to 400 KHz 01b=Module supports up to 1 MHz 10b=Reserved 11b=Reserved
	Reserved		Reserved
	Reserved		Reserved
3	Module state	03	Current state of Module 001b:ModuleLowPwr state(Flat memory passive cable assemblies)
	Interrupt		Digital state of IntL Interrupt output signal0b=IntL asserted1b=IntL not asserted (default)
4~7	Bank 0 lane flag	00	Indicates that one or more of the flag bits from bank 0
8	Reserved	00	Reserved
	Module state changed flag		Indicates change of Module state

9~13	Module Interrupt Flags	00	Module Interrupt Flags
14~25	Module monitors	00	Module monitors Temperature MSB
26~30	Module Global Controls	00	ForceLowPwr,Software Reset,Custom
31~36	Module Level Flag Masks	00	Module Level Flag Masks
37~63	Reserved	00	Reserved
64~84	Custom	00	Custom
85	Module Type Encodings	03	00h:Undefined01h:Optical Interfaces: MMF 02h:Optical interfaces: SMF 03h:Passive Cu 04h:Active Cable 005:Base-T
86	Module Host Electrical interface codes(ApSel:0001b)	1D	1A:100GBASE-CR4 NRZ 1D:400G CR8 PAM4
87	Module Media interface codes(ApSel:0001b)	01	01:Copper cable
88	Host/Media Lane Count(ApSel:0001b)	88	7-4:Host Lane Count 3-0:Media Lane Count

89	Lane Assignment(ApSel:0001b)	00	code 1:if application is allowed on a given host lane.bits0-7 correspond to host lanes 1-8
90	Module Host Electrical interface codes(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
91	Module Media interface codes(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
92	Host/Media Lane Count(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
93	Lane Assignment(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
94	Module Host Electrical interface codes(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
95	Module Media interface codes(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
96	Host/Media Lane Count(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
97	Lane Assignment(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
98	Module Host Electrical interface codes(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes

99	Module Media interface codes(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes
100	Host/Media Lane Count(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes
101	Lane Assignment(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes
102	Module Host Electrical interface codes(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
103	Module Media interface codes(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
104	Host/Media Lane Count(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
105	Lane Assignment(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
106	Module Host Electrical interface codes(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes
107	Module Media interface codes(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes
108	Host/Media Lane Count(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes

109	Lane Assignment(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes
110	Module Host Electrical interface codes(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
111	Module Media interface codes(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
112	Host/Media Lane Count(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
113	Lane Assignment(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
114	Module Host Electrical interface codes(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
115	Module Media interface codes(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
116	Host/Media Lane Count(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
117	Lane Assignment(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
118~125	Password Entry and Change	00	Password Entry and Change

126	Bank Select Byte	00	The module shall ignore the Bank Select byte if the Page Select byte is outside of the 10h to 1Fh range (inclusive).In this case the Bank Select byte shall revert to bank 0 and read/write operations shall be to bank 0.
127	Page Select Byte	00	Writing the value of a non-supported page shall not be accepted by the module. In such cases the Page Select byte shall revert to 0 and read/write operations shall be to upper page 00h.
128	Identifier	18	Identifier Type of Module
129~144	Vendor name	*	Vendor name(ASCII)
145	Vendor OUI	3C	Vendor IEEE company ID
146		18	
147		A0	
148~163	Vendor PN	*	Part number provided by vendor(ASCII)
164	Vendor rev	41	Vendor rev A
165		20	Vendor rev A

200	Module Card Power Class	00	000: Power class 1; 001: Power class 2010: Power class 3; 011: Power class 4100: Power class 5; 101: Power class 6110: Power class 7; 111: Power class 8
201	Max Power	06	Maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W
202	Cable assembly Length Lenth multiplier field	*	Multiplier for value in bits 5-0.00 = multiplier of .101 = multiplier of 110 = multiplier of 1011 = multiplier of 100
	Cable assembly Length Base Length field		Link length base value. To calculate actual link length use multiplier in bits 7-6.
203	Media connector Type	23	Type of connector present in the module.See SFF-8024 for codes.23h:Non-separable Connector
204	Copper cable Attenuation 5GHz	*	Passive copper cable attenuation at 5 GHz in 1 dB increments
205	Copper cable Attenuation 7GHz	*	Passive copper cable attenuation at 7 GHz in 1 dB increments
206	Copper cable Attenuation 12.89GHz	*	Passive copper cable attenuation at 12.89 GHz in 1 dB increments
207	Copper cable Attenuation 25.8GHz	*	Passive copper cable attenuation at 25.8 GHz in 1 dB increments
208	Reserved	00	Reserved

209	Reserved	00	Reserved
210	Near end implementation lane 8	00	0b=Lane 8 implemented in near end1b=Lane 8 not implemented in near end
211	Reserved	02	Reserved
	Implemented lanes in far end		See Table 27 for config code of discrete far end connectors
212	Media interface technology	0A	0A: Copper cable unequalized
213~220	Reserved	00	Reserved
221	Custom	00	Custom
222	Checksum	*	Include bytes 128-221
223~251	User custom info NV	00	User custom info NV
252~255	User custom info NV	00	User custom info NV

V. Bulk Cable Characteristics

The structure of the cable is shown as the figure , the characteristics of the bulk cable are listed below.
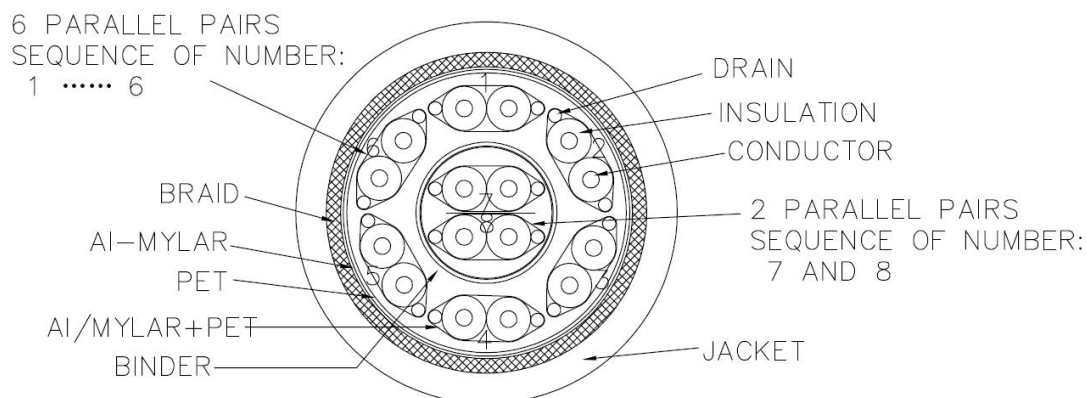
SECTIONAL DRAWING:

1. Voltage rating: 30V

2. Temperature rating: 80℃;

3. Impedance: Differential mode: 100 +5/-5 ohm @TDR;

4. Delay Skew(INTRA-SKEW): 30ps/5m max;

5. Signal Twin-ax pair cable: Solid Ag plated copper conductor;

6. Braid shielding coverage 85% min.

7. Jacket material: PVC

VI. Qualification Requirement Characteristics

ITEM		REQUIREMENT	TEST CONDITION
	Cable Impedance	100 +10/-5 Ω	
Differential Impedance	Paddle Card Impedance	100 ± 10 Ω	Rise time of 30ps(at the SMA) (20 % - 80 %)
	Cable Termination Impedance	100 +10 / -15 Ω	

|		
Differential (Input/Output)Return loss SDD11/SDD22	$\text{Return\_loss}(f) \geq \begin{cases} 16.5-2\sqrt{f} & 0.05 \leq f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{cases}$ Where f is the frequency in GHzReturn loss(f) is the return loss at frequency f	10MHz≤f ≤26.5GHz
Differential to common-mode (Input/Output)Return loss SCD11/SCD22	$\text{Return\_loss}(f) \geq \begin{cases} 22-(20/25.78)f & 0.01 \leq f < 12.89 \\ 15-(6/25.78)f & 12.89 \leq f \leq 19 \end{cases}$ Where f is the frequency in GHzReturn_loss(f) is the Differential to common-mode return loss at frequency f	10MHz≤f ≤26.5GHz
Common-mode to Common-mode (Input/Output)Return loss SCC11/SCC22	Return_loss(f)≥2dB 0.2≤f≤19 Where f is the frequency in GHz Return_loss(f) is the common-mode to common-mode return loss at frequency	10MHz≤f ≤26.5GHz
Differential Insertion Loss	(Differential InsertionLoss Max. For TPa to TPb Including Test fixture) Passive Cable : -17.16dB Min. @13.28GHz 	10MHz≤f ≤26.5GHz
Differential to common-mode Conversion Loss-Differential Insertion Loss(SCD21-SDD21)	$\text{Conversion\_loss}(f) - IL(f) \geq \begin{cases} 10 & 0.01 \leq f < 12.89 \\ 27-(29/22)f & 12.89 \leq f < 15.7 \\ 6.3 & 15.7 \leq f \leq 19 \end{cases}$ Where f is the frequency in GHz Conversion_loss(f) is the cable assembly differential to common-mode conversion loss IL(f) is the cable assembly insertion loss	10MHz≤f ≤26.5GHz
ICN	a is the IL@13.28GHz3 ≤ a ≤ 7.65: 9 mV Max7.65 ≤ a ≤ 26: 12.75 - 0.49 *a mV Max	10MHz≤f ≤26.5GHz
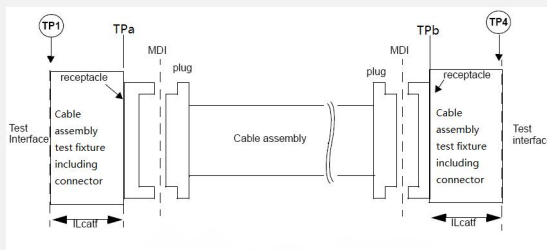
VII. Cable Assembly Characteristics

QSFP-DD TO 2QSFP56

Exploded View
1. Bot Back Shell
2. PCBA(QDD)
3. SUS304 LATCH
4. Top Back Shell
5. Heat Tube
6. Copper foil
7. Pull LATCH
8. Spring
9. Raw Cable
10. Lock LATCH

1. Bot Back Shell
2. PCBA(QSFP28)
3. SUS304 LATCH
4. Back Shell
5. SR
6. Copper foil
7. Pull LATCH
8. Spring
9. Raw Cable
10. Rivet
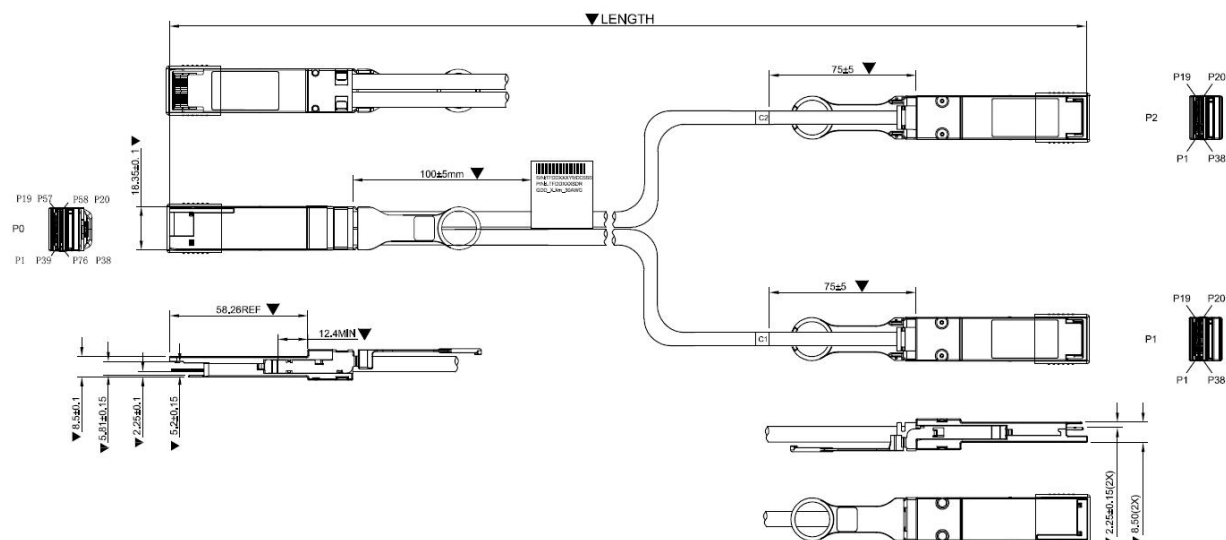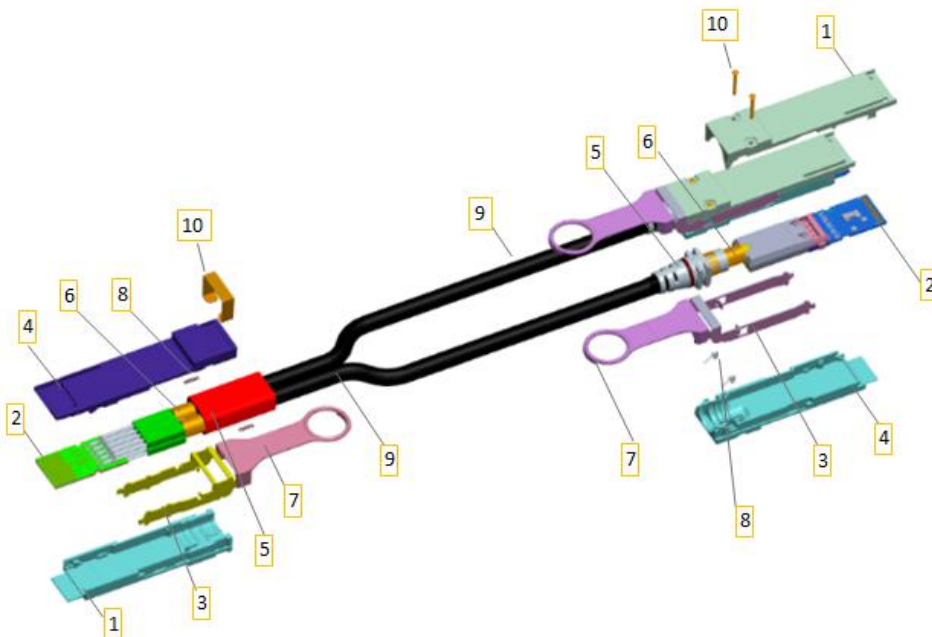
QSFP-DD 30AWG
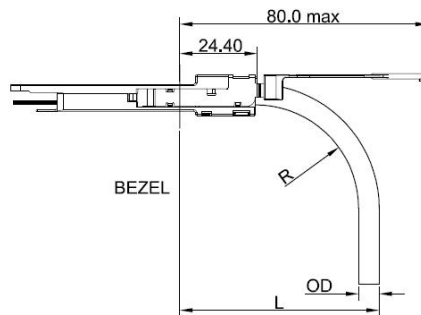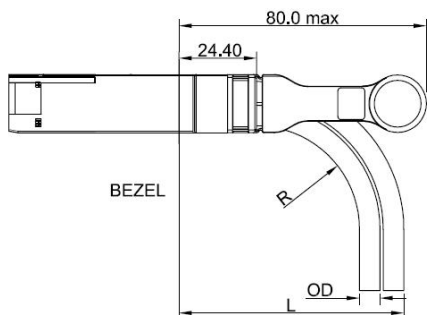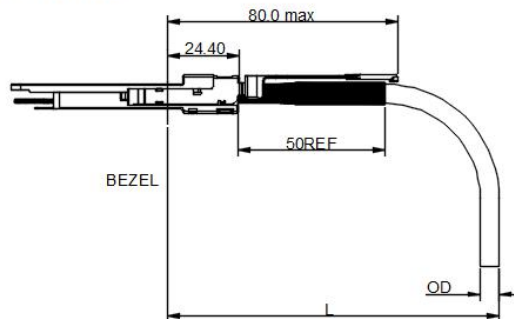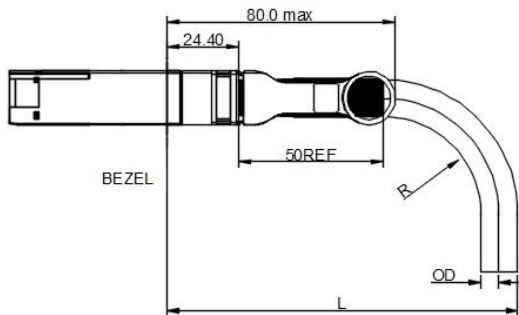
QSFP-DD Horizontal Direction			
CABLE GUAGE	DIAMETER "OD"	MIN.BEND RADIUS "R"	MIN.BEND SPACE "L"
30AWG	6.7MM	33.5MM	72MM

QSFP-DD Vertical Direction			
CABLE GUAGE	DIAMETER "OD"	MIN.BEND RADIUS "R"	MIN.BEND SPACE "L"
30AWG	6.7MM	33.5MM	65MM

QSFP-DD 28AWG

QSFP-DD Horizontal Direction			
CABLE GUAGE	DIAMETER "OD"	MIN.BEND RADIUS "R"	MIN.BEND SPACE "L"
28AWG	7.9MM	39.5MM	130MM

QSFP-DD Vertical Direction			
CABLE GUAGE	DIAMETER "OD"	MIN.BEND RADIUS "R"	MIN.BEND SPACE "L"
28AWG	7.9MM	39.5MM	122MM

FS

Test Center

FS.COM transceivers are tested to ensure connectivity and compatibility in our test center before shipped out. FS.COM test center is supported by a variety of mainstream original brand switches and groups of professional staff, helping our customers make the most efficient use of our products in their systems, network designs and deployments.
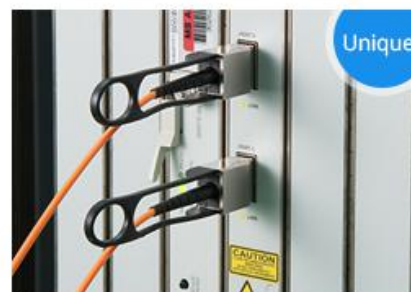
The original switches could be found nowhere but at FS.COM test center, eg: Juniper MX960 & EX 4300 series, Cisco Nexus 9396PX & Cisco ASR 9000 Series, HP 5900 Series & HP 5406R ZL2 V3(J9996A), Arista 7050S-64, Brocade ICX7750-26Q & ICX6610-48, Avaya VSP 7000 MDA 2, etc.

Cisco ASR 9000 Series(A9K-MPA-1X40GE)

ARISTA 7050S-64(DCS-7050S-64)

Juniper MX960

Brocade ICX 7750-26Q

Extreme Networks X670V VIM-40G4X

Mellanox M3601Q


Dell N4032F

HP 5406R ZL2 V3(J9996A)

AVAYA 7024XLS(7002QQ-MDA)

FS

Test Assured Program

FS.COM truly understands the value of compatibility and interoperability to each optics. Every module FS.COM provides must run through programming and an extensive series of platform diagnostic tests to prove its performance and compatibility. In our test center, we care of every detail from staff to facilities—professionally trained staff, advanced test facilities and comprehensive original-brand switches, to ensure our customers to receive the optics with superior quality.

Our smart data system allows effective product management and quality control according to the unique serial number, properly tracing the order, shipment and every part.
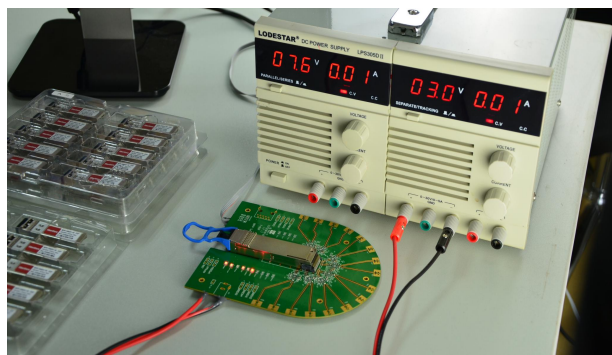
Our in-house coding facility programs all of our parts to standard OEM specs for compatibility on all major vendors and systems such as Cisco, Juniper, Brocade, HP, Dell, Arista and so on.

With a comprehensive line of original-brand switches, we can recreate an environment and test each optics in practical application to ensure quality and distance.

The last test assured step to ensure our products to be shipped with perfect package.

Order Information

Part Number	Data Rate	Length	Wire Gauge	Connector Type	Temp. Range	Cable Jacket
Q-2Q56PC005	Up to 400G	0.5m	30AWG	QSFP-DD to 2 QSFP56	0-70℃	PVC
Q-2Q56PC01	Up to 400G	1m	30AWG	QSFP-DD to 2 QSFP56	0-70℃	PVC
Q-2Q56PC02	Up to 400G	2m	28AWG	QSFP-DD to 2 QSFP56	0-70℃	PVC
Q-2Q56PC025	Up to 400G	2.5m	28AWG	QSFP-DD to 2 QSFP56	0-70℃	PVC

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United Kingdom
Russia
Germany
United States
China
Singapore
Australia

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The information in this document is subject to change without notice. FS has made all efforts to ensure the accuracy of the information, but all information in this document does not constitute any kind of warranty.