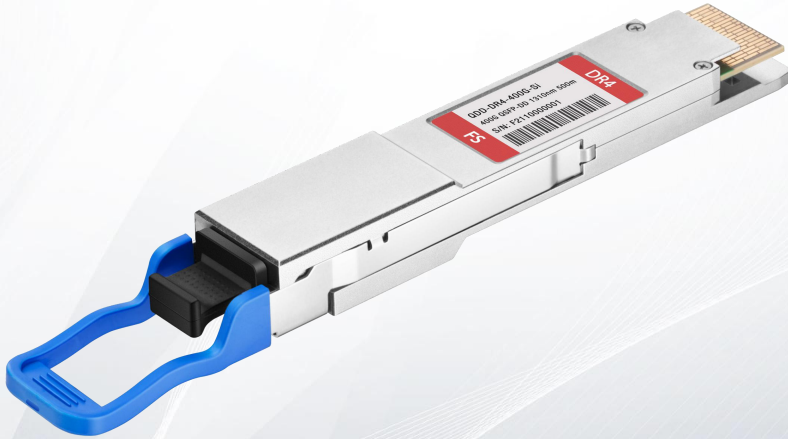**FS**

QSFP-DD 400GBASE-DR4 1310nm 500m Silicon Photonics Transceiver

QDD-DR4-400G-Si

Application

- 400G Ethernet
- InfiniBand Interconnects
- Data Center and Enterprise Networking

Features

- Compliant with QSFP-DD MSA
- Four Parallel 1310nm Optical Lanes
- IEEE 802.3bs 400GBASE-DR4 Specification Compliant
- Compliant with RoHS Requirement

- Up to 500m Transmission on Single Mode Fiber (SMF) with FEC
- 8x53.125Gb/s Electrical Interface (400GAUI-8)
- Data Rate 4*106.25Gbps (PAM4) Optical Interface

- Case Temperature Range: 0 to 70°C
- Maximum Power Consumption 10W
- MPO-12 Connector
- Built-in Digital Diagnostic Functions
- Laser Safety Class 1

Product Specifications

I. Absolute Maximum Ratings

Parameter	Unit	Min	Typ.	Max	Note
Storage Temperature	℃	-40		85	
Operating Relative Humidity	%	0		85	
Power Supply Voltage	V	-0.5		3.63	

II. Recommended Operating Conditions

Parameter	Unit	Min	Typ.	Max	Note
Storage Temperature	℃	0		70	
Power Supply Voltage	V	3.135	3.3	3.465	
Power Consumption	W			10	
Pre-FEC Bit Error Ratio			2.4E-4		
Post-FEC Bit Error Ratio			1E-12		1
Link Distance	m	2		500	2

Note:

1. FEC is provided by host system;

2. FEC is required on host system to support maximum distance.

III. Electrical Characteristics

Parameter	Unit	Min	Typ.	Max	Note
Transmitter					
Signaling Rate, each Lane	GBd		26.5625 ± 100 ppm		TP1
Data Input Swing Differential/TX	mV	85	-	1600	
Data Differential Impedance	Ω	90	100	110	
Receiver					
Signaling Rate, each Lane	GBd		26.5625 ± 100 ppm		TP4
Data Output Swing Differential/RX	mV		-	900	
Data Differential Impedance	Ω	90	100	110	

IV. Optical Characteristics (Under the Recommended Operating Environment)

Parameter	Unit	Min	Typ.	Max	Note
Transmitter					
Signaling rate, each lane	GBd		53.125 ± 100 ppm		PAM4
TX Central Wavelength	nm	1304.5	1310	1317.5	
Side-mode Suppression Ratio (SMSR)	dB	30			
Average Launch Power, each lane	dBm	-2.9		4	1
Outer Optical Modulation Amplitude (OMAouter), each lane	dBm	-0.8		4.2	2

Parameter	Unit	Min	Typ.	Max	Note
Launch Power in OMAouter minus TDECQ, each Lane(min)	dBm	-2.2			
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane (max)	dB			3.4	3
Average Launch Power of OFF Transmitter, each lane (max)	dBm			-15	
Extinction Ratio, each lane (min)	dB	3.5			
Optical Return Loss Tolerance (max)	dB			21.4	
RIN21.4OMA (max)	dB/Hz			-136	
Transmitter Reflectance (max)	dB			-26	

Receiver

| Parameter	Unit	Min	Typ.	Max	Note
Signaling Rate, each lane	Gbps		53.125 ± 100 ppm		PAM4
RX Central Wavelength	nm	1304.5	1310	1317.5	
Damage Threshold (min)	dBm	5			4
Average Receive Power per Lane	dBm	-5.9		4.0	5
Receiving Power (OMAouter) per Lane	dBm			4.2	
Receiver Reflectance (max)	dB			-26	
Receiver Sensitivity (OMAouter), each lane (max)	dBm		Equation (1)		6
Stressed Receiver Sensitivity (OMAouter) per Lane	dBm			-1.9	7

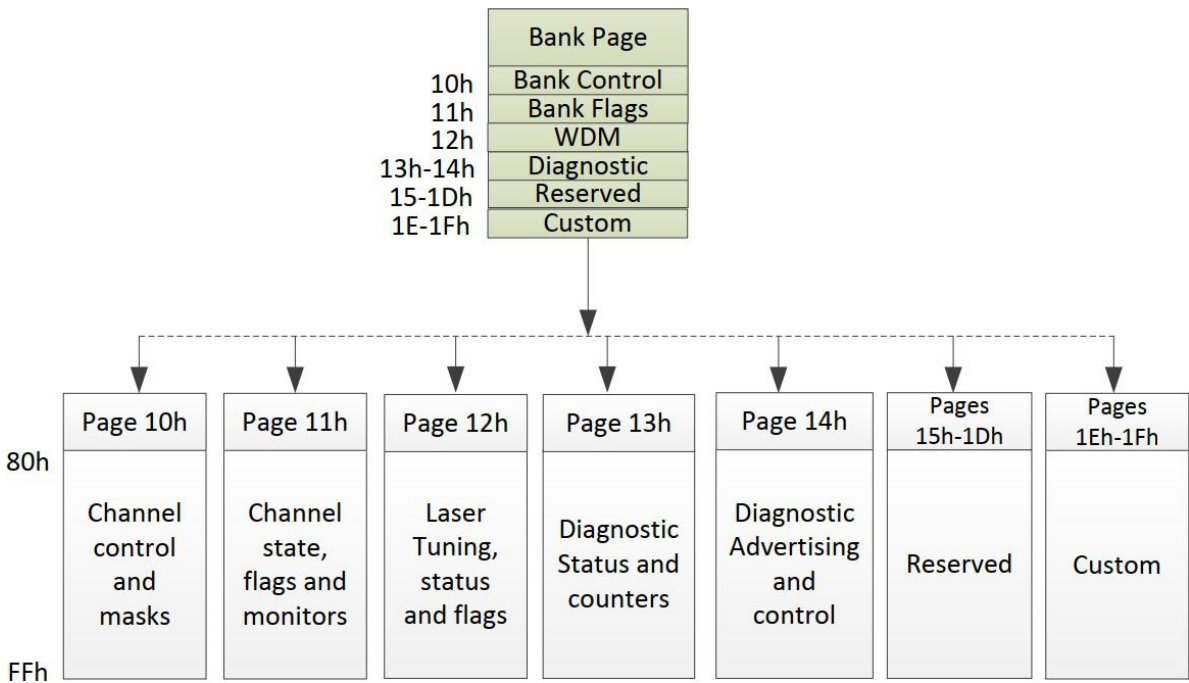| Parameter	Unit	Min.	Typ.	Max.	Note
Conditions of Stressed Receiver Sensitivity Test					
Stressed Eye Closure for PAM4 (SECQ), lane under test	dB		3.4		8
OMAouter of each aggressor lane	dBm			4.2	
LOS Assert	dBm	-15			
LOS De-Assert	dBm			-8.9	
LOS Hysteresis	dB	0.5			

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance;

2. Even if the TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or TDECQ < 1.1dB for an extinction ratio of < 5dB, the OMAouter (min) must exceed the minimum value specified here;

3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement;

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance;

5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power;

6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation: RS=max (−3.9, SECQ−5.3), where RS is the receiver sensitivity, and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity. which is illustrated in the Figure;
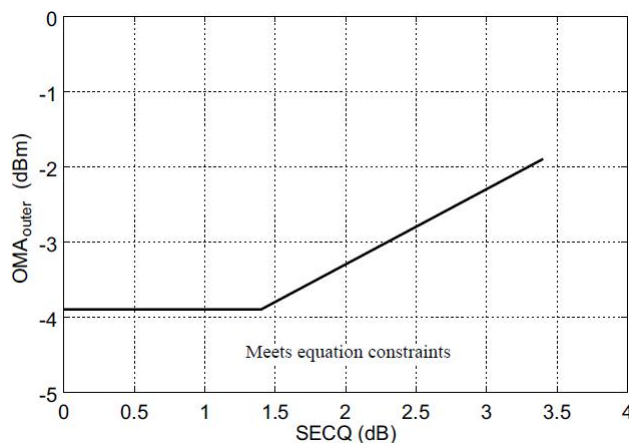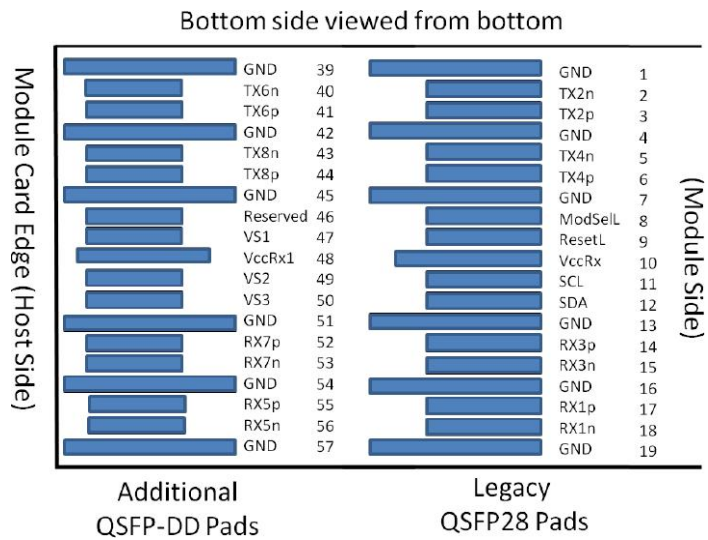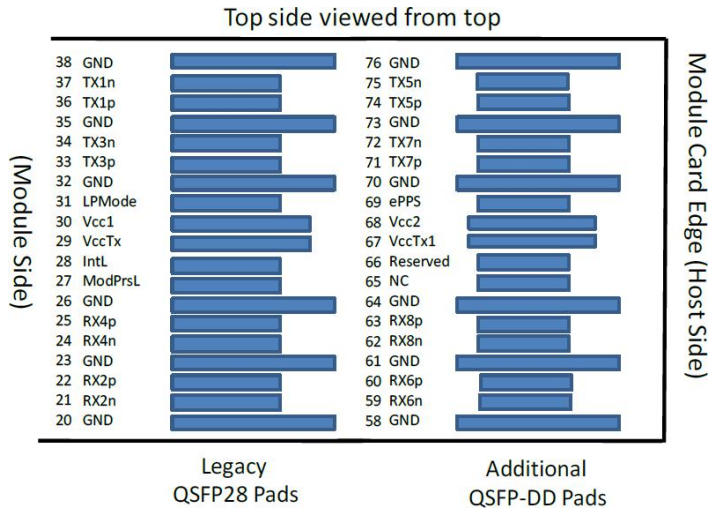

7. Measured with conformance test signal at TP3 for the BER equal to 2.4E-4;

8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

V. Digital Diagnostic Functions

Parameter	Unit	Error	Note
Temperature Monitor	℃	±3	1LSB=1/256℃
Supply Voltage Monitor	V	±0.1	1LSB=100uV
Bias Current Monitor	mA	±10%	1LSB=2uA
TX Power Monitor	dBm	±3	1LSB=0.1uW
RX Power Monitor	dBm	±3	1LSB=0.1uW

VI. Pin Assignment and Description

Top side viewed from top

38	GND	76	GND
37	TX1n	75	TX5n
36	TX1p	74	TX5p
35	GND	73	GND
34	TX3n	72	TX7n
33	TX3p	71	TX7p
32	GND	70	GND
31	LPMode	69	ePPS
30	Vcc1	68	Vcc2
29	VccTx	67	VccTx1
28	IntL	66	Reserved
27	ModPrsL	65	NC
26	GND	64	GND
25	RX4p	63	RX8p
24	RX4n	62	RX8n
23	GND	61	GND
22	RX2p	60	RX6p
21	RX2n	59	RX6n
20	GND	58	GND

(Module Side) — Module Card Edge (Host Side)

Legacy QSFP28 Pads — Additional QSFP-DD Pads

Bottom side viewed from bottom

GND	39	GND	1
TX6n	40	TX2n	2
TX6p	41	TX2p	3
GND	42	GND	4
TX8n	43	TX4n	5
TX8p	44	TX4p	6
GND	45	GND	7
Reserved	46	ModSelL	8
VS1	47	ResetL	9
VccRx1	48	VccRx	10
VS2	49	SCL	11
VS3	50	SDA	12
GND	51	GND	13
RX7p	52	RX3p	14
RX7n	53	RX3n	15
GND	54	GND	16
RX5p	55	RX1p	17
RX5n	56	RX1n	18
GND	57	GND	19

Module Card Edge (Host Side) — (Module Side)

Additional QSFP-DD Pads — Legacy QSFP28 Pads

Pad	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	

Pad	Logic	Symbol	Description	Plug Sequence	Notes
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	

Pad	Logic	Symbol	Description	Plug Sequence	Notes
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power Supply Transmitter	2B	2
30		Vcc1	+3.3V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization Mode; In legacy QSFP applications, the InitMode pad is calledLPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1

Pad	Logic	Symbol	Description	Plug Sequence	Notes
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3

Pad	Logic	Symbol	Description	Plug Sequence	Notes
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal- common ground plane;

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA;

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF;

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.
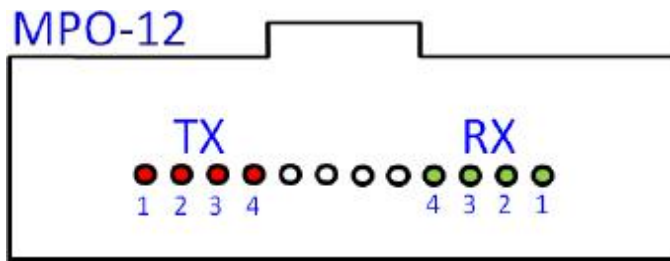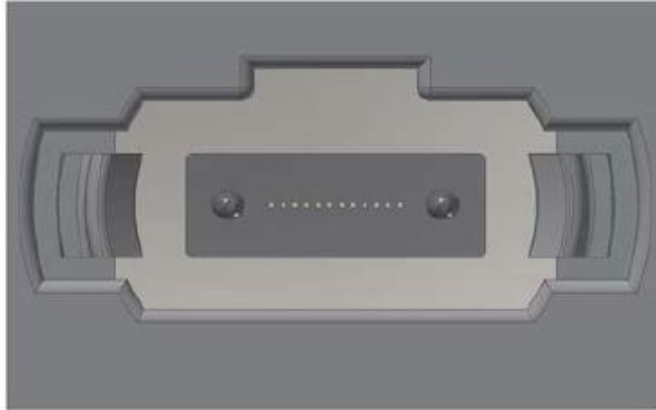
VII. Recommended Power Supply Filter
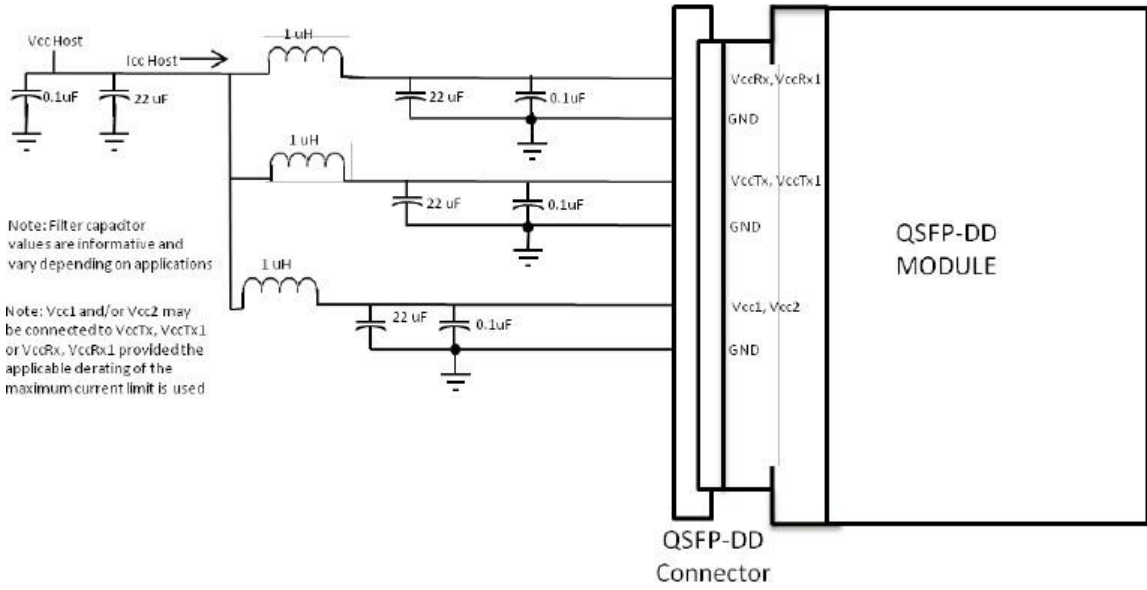
VIII. Mechanical Outlines
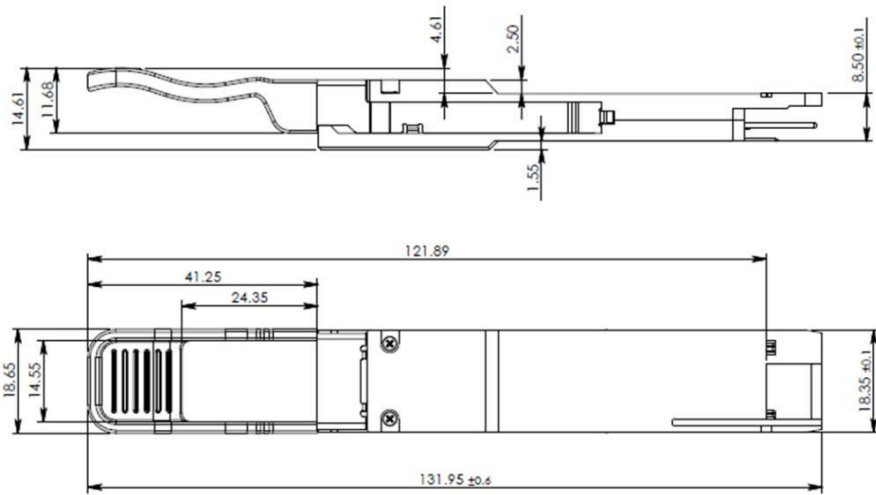
IX. Optical Interface

X. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

XI. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Test Center

FS.COM transceivers are tested to ensure connectivity and compatibility in our test center before shipped out. FS.COM test center is supported by a variety of mainstream original brand switches and groups of professional staff, helping our customers make the most efficient use of our products in their systems, network designs and deployments.

The original switches could be found nowhere but at FS.COM test center, eg: Juniper MX960 & EX 4300 series, Cisco Nexus 9396PX & Cisco ASR 9000 Series, HP 5900 Series & HP 5406R ZL2 V3(J9996A), Arista 7050S-64, Brocade ICX7750-26Q & ICX6610-48, Avaya VSP 7000 MDA 2, etc.

Cisco ASR 9000 Series(A9K-MPA-1X40GE)

ARISTA 7050S-64(DCS-7050S-64)

Juniper MX960

Brocade ICX 7750-26Q

Extreme Networks X670V VIM-40G4X

Mellanox M3601Q

Dell N4032F

HP 5406R ZL2 V3(J9996A)

AVAYA 7024XLS(7002QQ-MDA)

Test Assured Program

FS.COM truly understands the value of compatibility and interoperability to each optics. Every module FS.COM provides must run through programming and an extensive series of platform diagnostic tests to prove its performance and compatibility. In our test center, we care of every detail from staff to facilities—professionally trained staff, advanced test facilities and comprehensive original-brand switches, to ensure our customers to receive the optics with superior quality.

Our smart data system allows effective product management and quality control according to the unique serial number, properly tracing the order, shipment and every part.
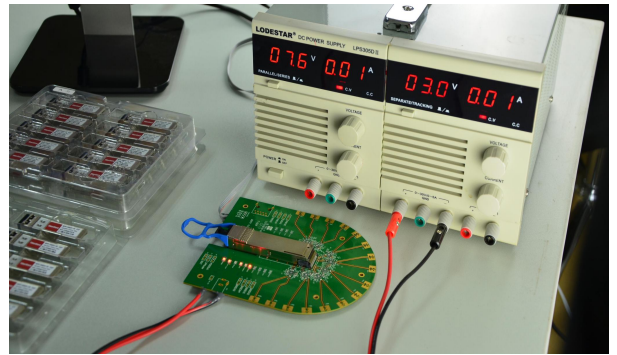
Our in-house coding facility programs all of our parts to standard OEM specs for compatibility on all major vendors and systems such as Cisco, Juniper, Brocade, HP, Dell, Arista and so on.

With a comprehensive line of original-brand switches, we can recreate an environment and test each optics in practical application to ensure quality and distance.

The last test assured step to ensure our products to be shipped with perfect package.

Order Information

Part Number	Description
QSFPDD-SR8-400G	QSFP-DD 400GBASE-SR8 850nm 100m Transceiver
QSFPDD-DR4-400G	QSFP-DD 400GBASE-DR4 1310nm 500m Transceiver
QDD-DR4-400G-Si	QSFP-DD 400GBASE-DR4 1310nm 500m Silicon Photonics Transceiver
QSFPDD-XDR4-400G	QSFP-DD 400GBASE-DR4+ 1310nm 2km Transceiver
QSFPDD-FR4-400G	QSFP-DD 400GBASE-FR4 1310nm 2km Transceiver
QSFPDD-LR4-400G	QSFP-DD 400GBASE-LR4 1310nm 10km Transceiver
QSFPDD-LR8-400G	QSFP-DD 400GBASE-LR8 1310nm 10km Transceiver

Note:

400G QSFP-DD transceiver module is individually tested on corresponding equipment such as Cisco, Arista, Juniper, Dell, Brocade and other brands, and passes the monitoring of FS.COM intelligent quality control system.

FS

United Kingdom   Russia

Germany

United States

China

Singapore

Australia

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