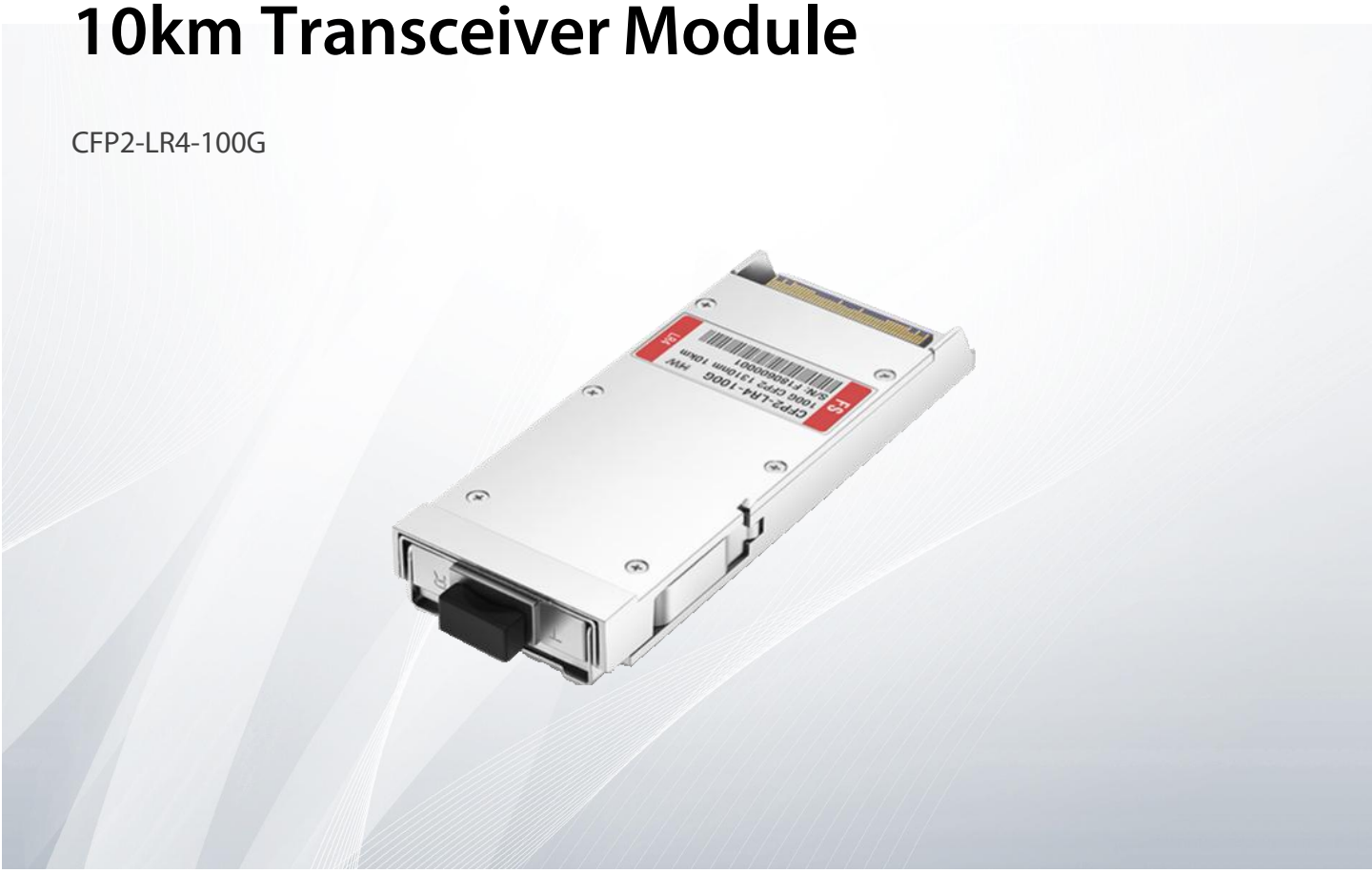
CFP2 100GBASE-LR4 1310nm 10km Transceiver Module

CFP2-LR4-100G



Application

- 100GE Routers and Switches
- 100G OTN
- 100G Network Security And Monitoring

Features

- Hot Pluggable CFP2 MSA package
- IEEE 802.3ba 100GBASE-LR4 compliant
- CFP2 MSA Compliance
- ITU-T G.959.1 2012
- Up to 10km for G.652 SMF
- Cooled 4x25G LAN-WDM transmitter
- 4 x 28G Electrical Serial Interface (CEI-28G-VSR)
- MDIO management interface with Digital Diagnostic
- +3.3V power supply
- Power consumption less than 6W
- Compact size: 107.5×41.5×12.4 mm
- Operating case temperature: -5 to +70 ℃
- Duple LC Receptacle
- ROHs-6 compliant

Description

FS's CFP2-100G-LR4 transceivers are designed for use in 100 Gigabit Ethernet links over 10km single module fiber, and it compliant to the CFP MSA CFP2 HW Specification and IEEE 802.3ba 100GBASE-LR4. Digital diagnostics are available via MDIO as specified in the CFP MSA Management Interface Specification.

The transceiver's designs are optimized for high performance and cost efficiency to provide customers the best solutions for Datacom and Telecom applications.

The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

Product Specifications

I. Absolute Maximum Ratings

The limit of the maximum value is shown as below Table 1. (If operating out the limit of the maximum value will cause permanent damage).

Parameter	Symbol	Conditions	Min.	Max	Unit	Ref.
Storage temperature(case)	Tstg		-40	+85	℃	
Relative humidity	RH	0		85	%	
Damage Threshold for Receiver	Pmax			+10.0	dBm	
Power Supply	Vcc3.3V		-0.3	+3.6	V	
	Vcc5.0V				V	
Input 3.3V LVCMOS signal level	Vi		-0.3	Vcc+0.3	V	
Input 1.2V LVCMOS signal level	Vi		-0.3	1.6	V	
ESD Sensitivity on module and all host pins	HBM	Human Body model R=1.5K,C=100pF		2000	V	

II. Recommended Operating Environment

The recommended working conditions are shown as below Table 2.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Operating Case Temperature	Tc	0		+70	℃	
Supply voltage	Vcc 3.3V	+3.14	+3.3	+3.47	V	
Power dissipation	P			6	W	
Low Power dissipation	PLow			1	W	
In-rush Curent	I-inrush			200	mA/us	
Turn-off rush Curent	I-turnoff	-200			mA/us	
Link Distance	L	2M		10km	G.652 SMF	

III. Optical Characteristics

Table 3 -100Gb/s CFP2 Optical Specifications (100GBase-LR4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter						
Channel data rate				25.7812		Gbps
Aggregate data rate				103.125		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout				10.5	dBm
Average Launch Power per Lane	Peach		-4.3		4.5	dBm

Optical Modulation Amplitude per Lane	OMA		-1.3		4.5	dBm
Difference in Launch power between any two lances(OMA)					5.0	dB
Launch power in OMA minus TDP, per lane	Poma tdp		-2.3			dBm
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H			-30	dBm
Extinction Ratio	ER		4			dB
SMSR	SMSR		30			dB
Dispersion Penalty	DP	10km SMF			2.2	dB
Relative Intensity Noise	RIN	Mod off			-130	dB/Hz
Opitcal Return Loss Tolerance	TRL				20	dB
Transmitter reflectance	Tef				-12	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}1	EM		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}			
			Receiver			
Channel data rate				25.7812		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Damage threshold	PDT			5.5		dBm
Average receiver power per lane	Rpow		-10.6		4.5	dBm
Receive power OMA per Lane	Rovl				4.5	dBm
Difference in receive power between any two lanes(OMA)					5.5	dB
Receiver Sensitivity(OMA) per lane	Psen				-8.6	dBm

Stressed Receiver Sensitivity per Lane	Psen_str				-6.8	dBm
Receiver Reflectance	Ref				-26	dB
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty per Lane					1.8	dB
Stressed eye jitter per Lane					0.3	UI
Rx-Lane LOS Assert			-25			dBm
Rx-Lane LOS De-assert					-13	dBm
Rx-Lane LOS Hysteresis			0.5			dB

Note1. Please refer to Figure 1

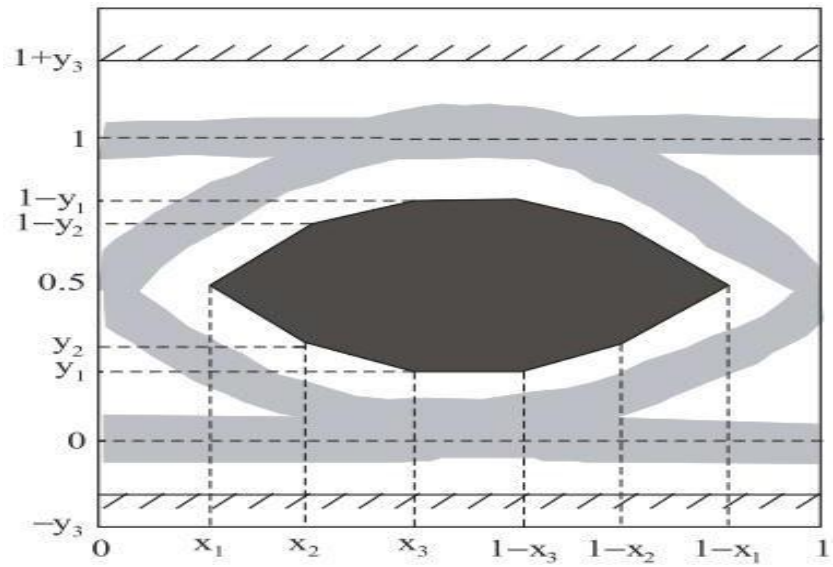


Figure 1 - Transmission eye mask definition

Table 4 -100Gb/s CFP2 Optical Specifications (OTU4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter						
Channel data rate				27.9525		Gbps
Aggregate data rate				111.809		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	λcT0		1294.53	1295.56	1296.59	nm
	λcT1		1299.02	1300.05	1301.09	nm
	λcT2		1303.54	1304.58	1305.63	nm
	λcT3		1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout				8.9	dBm
Average Launch Power per Lane	Peach		-2.5		2.9	dBm
Optical Modulation Amplitude per Lane	OMA		-1.2		4.5	dBm
Difference in Launch power between any two lances(OMA)					5.0	dB
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H			-30	dBm
Extinction Ratio	ER		7			dB
SMSR	SMSR		30			dB
Relative Intensity Noise	RIN	Mod off			-130	dB/Hz
Opitcal Return Loss Tolerance	TRL				20	dB
Transmitter reflectance	Tef				-12	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}[1]	EM		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}			

Receiver

Channel data rate				27.9525		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	λcR0		1294.53	1295.56	1296.59	nm
	λcR1		1299.02	1300.05	1301.09	nm
	λcR2		1303.54	1304.58	1305.63	nm
	λcR3		1308.09	1309.14	1310.19	nm
Damage threshold	PDT			5.5		dBm
Average receiver power per lane	Rpow				4.5	dBm
Receiver power OMA per lane	Rovl				4.5	dBm
Difference in receive power between any two lanes(OMA)					5.5	dB
Optical path penalty					1.5	dB
Receiver Sensitivity per lane[2]	Psen				-10.3	dBm
Receiver Sensitivity(OMA) per lane[2]	Psen_OMA				-9.1	dBm
Receiver Reflectance	Ref				-26	dB
Rx-Lane LOS Assert			-25			dBm
Rx-Lane LOS Deassert					-13	dBm
Rx-Lane LOS Hysteresis			0.5			dB

Note1. Please refer to Figure 1
Note2. OTU-4 Rate, BER < 10-12 with FEC, ER > 7dB

IV. Electrical Characteristics

Table 5 - 100Gb/s CFP2 Electrical High Speed I/O Interface Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter (CAUI input interface)						
Signal Rate Per Lane				25.78125		Gb/s
Signal Rate Tolerance			-100		100	ppm
AC Common Mode inputVoltage Tolerance(RMS)					20	mV
Differential input returnloss	RI_{diff}	IEEE 802.3ba-2010	See Equation (83B–7)			dB
Total Input Jitter Tolerance	T_{jin}				0.62	UI
Deterministic Input Tolerance -Jitter	T_{din}				0.42	UI
Transmitter Input Mask (X1, X2)-Eye			(0.31, 0.5)			UI[1]
Transmitter Input Mask (Y1, Y2)-Eye			(42.5, 425)			mV[1]
Receiver (CAUI output interface)						
Signal Rate Per Lane				25.78125		Gb/s
Signal Rate Tolerance			-100		100	ppm
Single-ended output voltage	Vosig		-0.4		4	V
Output AC common-modevoltage(RMS)	VocomAC				15	mV
Output transition time	Tr	20%~80%	24			ps
Differential output returnloss		IEEE802.3ba-2010	See Equation (83B–5)			dB
Total Jitter	Tj				0.4	UI
Deterministic Jitter	Tdj				0.25	UI

Receiver Output Eye Mask(X1, X2)				(0.2,0.5)	UI[2]
Receiver Output Eye Mask(Y1, Y2)				(136,380)	mV[2]

Note1. refer to figure 2
Note2. refer to figure 3

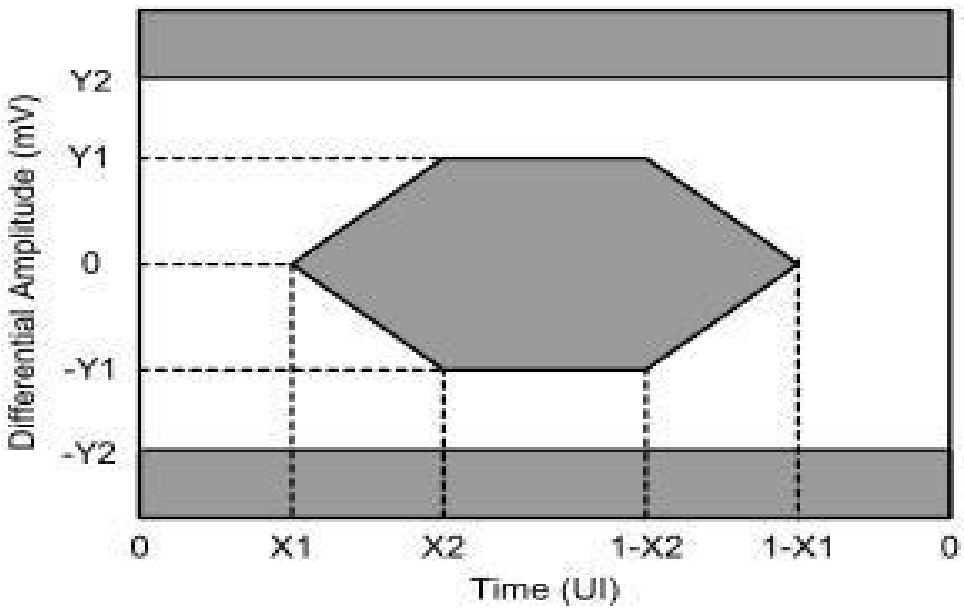


Figure 3 - CAUI transmitter eye mask

Low Speed I/O interface

Table 6 -100Gb/s CFP2 3.3V LVCMOS Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc		3.2	3.3	3.4	V
Input High Voltage	V_{IH}		2		Vcc+0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input Leakage Current	I_{IN}		-10		+10	mA
Output High Voltage (IOH =-100uA)	V_{OH}		Vcc-0.2		Vcc+0.3	V

Output Low Voltage (IOL =100uA)	V_{OL}		-0.3		0.2	V
Minimum Pulse Width of Control Pin Signal	t_CNTL		100			us

Note:(MOD_RSTn,MOD_LOPWR,TX_DIS,PRG_CNTL,MOD_ABS,RX_LOS,GLB_ALRMn, PRG_ALRM) are LVCMOS I/O interfaces.

Table 7 - 100Gb/s CFP 1.2V LVCMOS Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input High Voltage	VI_H		0.84		1.5	V
Input Low Voltage	V_{IL}		-0.3		0.36	V
Input Leakage Current	I_{IN}		-100		+100	uA
Output High Voltage	V_{OH}		1.0		1.5	V
Output Low Voltage	V_{OL}		-0.3		0.2	V
Output High Current	I_{OH}				-4	mA
Output Low Current	I_{OL}		+4			mA
Input capacitance	C_i				10	pF

Note:(MDIO, MDC, PRTADR4:0) are 1.2V LVCMOS I/O interfaces

Table 8 - 100Gb/s CFP Timing Parameters for CFP2 Hardware Signal Pins

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
HardwareMOD_LOPWR assert	t_MOD_LOPWR_assert				1	ms
Hardware MOD_LOPWR De-assert	t_MOD_LOPWR_deassert				10	s
Receiver Loss of Signal Assert Time	t_loss_assert				100	us

Receiver Loss of Signal De-Assert Time	t_loss_deassert				100	us
Global Alarm Assert Delay Time	GLB_ALRMn_assert				150	ms
Global Alarm De-AssertDelay Time	GLB_ALRMn_deassert				150	ms
Management Interface ClockPeriod	t_prd		250			ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP MDIO t_delay	t_delay		0		175	ns
Initialization time from Reset	t_initialize				2.5	s
Transmitter Disabled(TX_DIS asserted)	t_de-assert				100	us
Transmitter Enabled(TX_DIS de-asserted)	t_assert				2	ms

Table 9 - 100Gb/s CFP MDIO and MDC Timing Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Management Interface Clock Frequency	F_MDC		0.1		4	MHz
Management Interface Clock Period	t_prd		250		10000	ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP MDIO t_delay1	t_delay		0		175	ns
MDC high and low time	twidth		40		60	%
			160			ns
MDIO/MDC termination in CFP	Zt		100			kOhm

Note1. Delay from MDC rising edge to MDIO data change

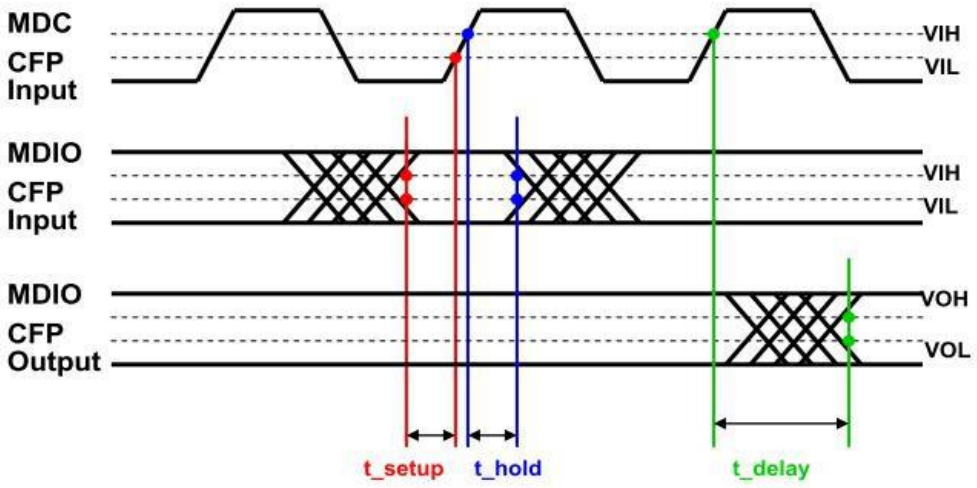


Figure 4 -100Gb/s CFP MDIO & MDC Timing Diagram

Clock interface

Table 10 - 100Gb/s CFP Reference Clock Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Impedance	Zd		80	100	120	ohm
Frequency			1/64 of host lane rate			
Frequency Stability	Xf		-100		+100	ppm[1]
			-20		+20	ppm[2]
Input Differential Voltage	Vdiff		400		1200	mV[3]
RMS Jitter	σ				10	ps[4]
Clock Duty Cycle			40		60	%
Clock Rise/Fall Time 10/90%	Tr/f		200		1250	ps[5]

Note1. For Ethernet applications **Note2.** For Telecom applications
Note3. Peak to Peak Differential
Note4. Random Jitter. Over frequency band of 10kHz < f < 10MHz
Note5. 1/64 of electrical lane

Table 11 - 100Gb/s CFP Transmitter & Receiver Monitor Clock Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Impedance	Zd		80	100	120	ohm
Frequency			1/8 of network lane rate			
Ouput Differential Voltage	Vdiff		400		1200	mV[1]
Clock Duty Cycle			40		60	%

Note1. Peak to Peak Differential

V. 100Gb/s CFP Function Diagram

Internal reference structure

The internal structure of 100Gb/s CFP shown as Figure 5.

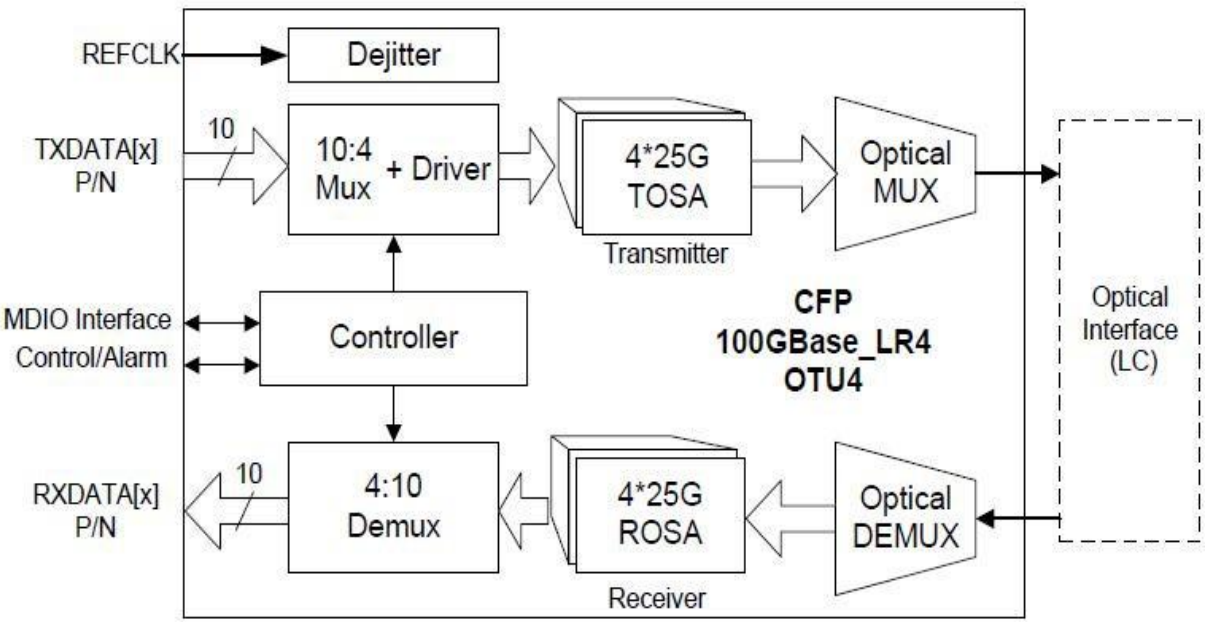


Figure 5 -10km 100Gb/s CFP2 internal structure

VI.Recommended Interface Circuit

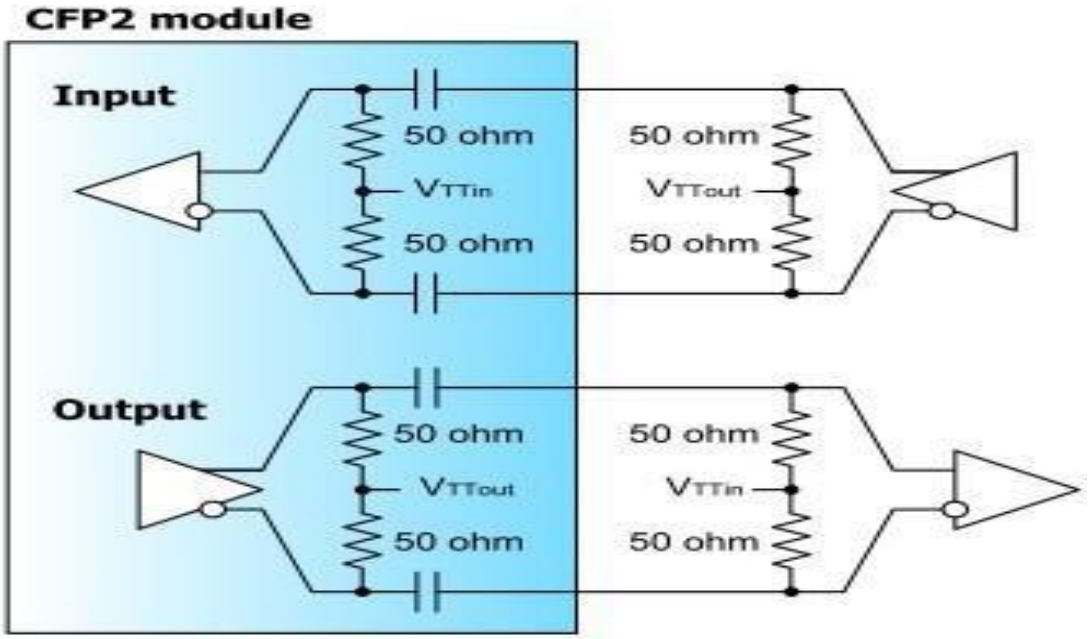


Figure 6 - Recommended High Speed I/O for Data and Clocks

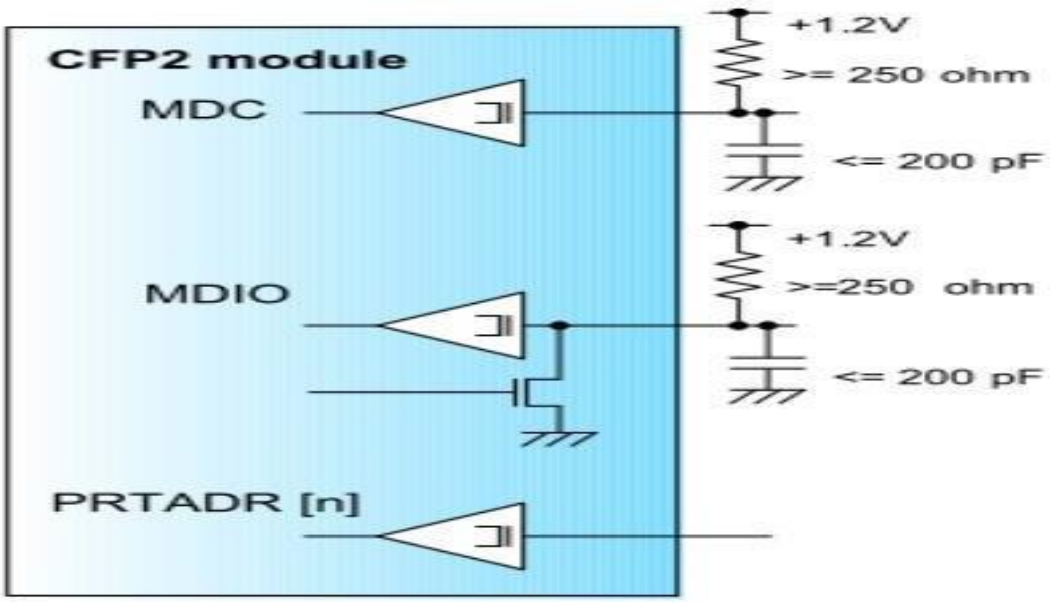


Figure 7 - Recommended MDIO Interface Termination

VII.Pin Layout

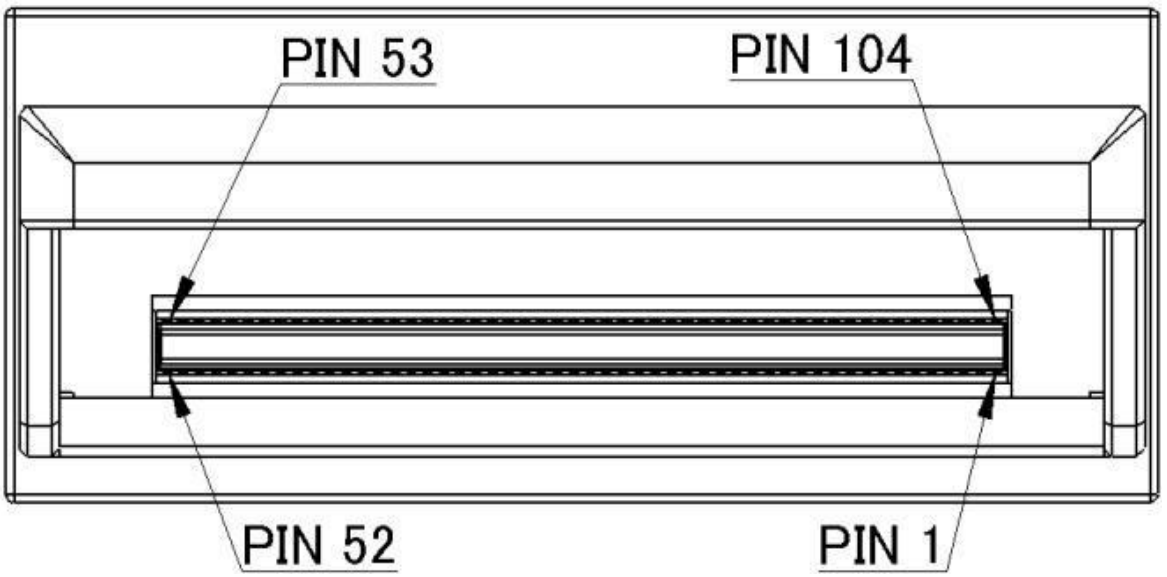
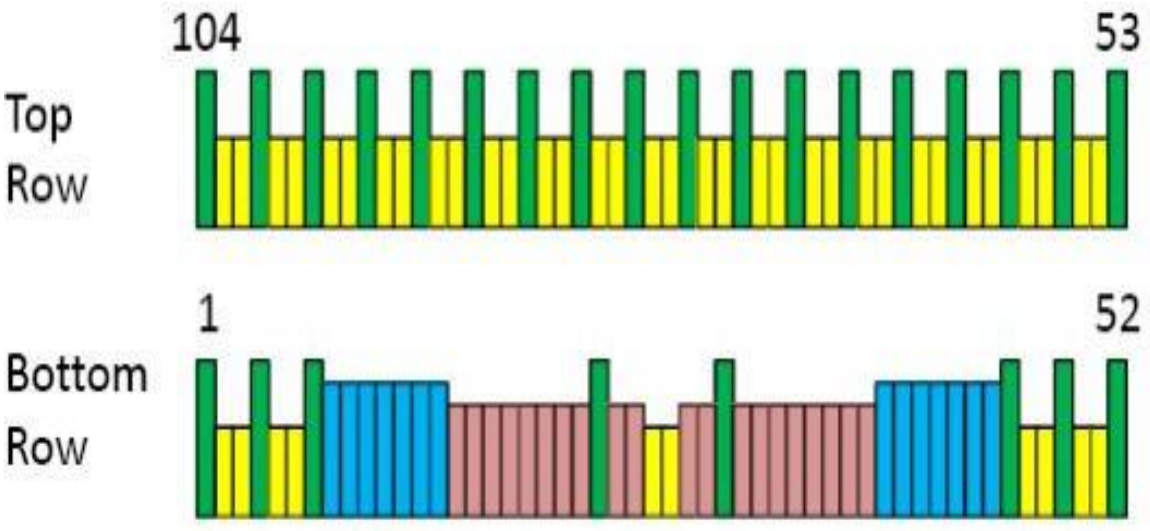


Figure 8 - CFP2 Module Pad Layout



	CFP2 Bottom		CFP2 Top
1	GND	104	GND
2	(TX_MCLKn)	103	N.C.
3	(TX_MCLKp)	102	N.C.
4	GND	101	GND
5	N.C.	100	TX3n
6	N.C.	99	TX3p
7	3.3V_GND	98	GND
8	3.3V_GND	97	TX2n
9	3.3V	96	TX2p
10	3.3V	95	GND
11	3.3V	94	N.C.
12	3.3V	93	N.C.
13	3.3V_GND	92	GND
14	3.3V_GND	91	N.C.
15	VND_IO_A	90	N.C.
16	VND_IO_B	89	GND
17	PRG_CNTL1	88	TX1n
18	PRG_CNTL2	87	TX1p
19	PRG_CNTL3	86	GND

20	PRG_ALRM1	85	TX0n
21	PRG_ALRM2	84	TX0p
22	PRG_ALRM3	83	GND
23	GND	82	N.C.
24	TX_DIS	81	N.C.
25	RX_LOS	80	GND
26	MOD_LOPWR	79	(REFCLKn)
27	MOD_ABS	78	(REFCLKp)
28	MOD_RSTn	77	GND
29	GLB_ALRMn	76	N.C.
30	GND	75	N.C.
31	MDC	74	GND
32	MDIO	73	RX3n
33	PRTADR0	72	RX3p
34	PRTADR1	71	GND
35	PRTADR2	70	RX2n
36	VND_IO_C	69	RX2p
37	VND_IO_D	68	GND
38	VND_IO_E	67	N.C.
39	3.3V_GND	66	N.C.
40	3.3V_GND	65	GND

41	3.3V	64	N.C.
42	3.3V	63	N.C.
43	3.3V	62	GND
44	3.3V	61	RX1n
45	3.3V_GND	60	RX1p
46	3.3V_GND	59	GND
47	N.C.	58	RX0n
48	N.C.	57	RX0p
49	GND	56	GND
50	(RX_MCLKn)	55	N.C.
51	(RX_MCLKp)	54	N.C.
52	GND	53	GND

Figure 8 - CFP2 Module Pin Map

Note1: Pin 15,16,36,37,38, are internally used and NOT allowed to connect any signal and power supply or GND
Note2: Pin 2,3,50,51 are disabled unless MCLK output is enabled via MDIO

VIII.Pin Definition

Table 12 - 100Gb/s CFP2 Pin Definition(Bottom raw)

PIN	Name	I/O	Logic	Description
1	GND			
2	(TX_MCLKn)	O	CML	Not Support
3	(TX_MCLKp)	O	CML	Not Support
4	GND			

5	N.C			No Connect
6	N.C			No Connect
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage
11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O. Must No Connect at host board
16	VND_IO_B	I/O		Module Vendor I/O. Must No Connect at host board
17	PRG_CNTL1	I	LVCMOSw/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used4.75kohm pull up in the module
18	PRG_CNTL2	I	LVCMOSw/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01":≤6W, "10": ≤9W, "11" or NC: ≤12W = not used4.75kohm pull up in the module
19	PRG_CNTL3	I	LVCMOSw/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤3W, "01":≤6W, "10": ≤9W, "11" or NC: ≤12W = not used 4.75kohm pull up in the module

20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0":module not high powered up
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default:MOD_READY, "1": Ready, "0": not Ready.
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND			
24	TX_DIS	I	LVCMOSw/ PUR	Transmitter Disable for all lanes,"1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low opticalsignal, "0": normal condition
26	MOD_LOPWR	I	LVCMOSw/ PUR	Module Low Power Mode."1" or NC: module in low power (safe) mode, "0": power-on enabled4.75kohm pull up in the module
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0":module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOSw/ PDR	Module Reset. "0" resets the module, "1" or NC =module enabled, 4.75kohm pull down in the module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)

32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	N.C			No Connect
48	N.C			No Connect
49	GND			
50	(RX_MCLKn)	O	CML	Not Support

51	(RX_MCLKp)	O	CML	Not Support
52	GND			

Table 13 -100Gb/s CFP2 Pin Definition(Top raw)

PIN	Name	I/O	Logic	Description
53	GND			
54	N.C			No Connect
55	N.C			No Connect
56	GND			
57	RX0p	O	HS I/O	Lane 0 Receiver Output (Positive)
58	RX0n	O	HS I/O	Lane 0 Receiver Output (Negative)
59	GND			
60	RX1p	O	HS I/O	Lane 1 Receiver Output (Positive)
61	RX1n	O	HS I/O	Lane 1 Receiver Output (Negative)
62	GND			
63	N.C			No Connect
64	N.C			No Connect
65	GND			
66	N.C			No Connect
67	N.C			No Connect
68	GND			
69	RX2p	O	HS I/O	Lane 2 Receiver Output (Positive)

70	RX2n	O	HS I/O	Lane 2 Receiver Output (Negative)
71	GND			
72	RX3p	O	HS I/O	Lane 3 Receiver Output (Positive)
73	RX3n	O	HS I/O	Lane 3 Receiver Output (Negative)
74	GND			
75	N.C			No Connect
76	N.C			No Connect
77	GND			
78	REFCLKp	I		Reference Clock Input (Positive), optional
79	REFCLKn	I		Reference Clock Input (Negative) , optional
80	GND			
81	N.C			No Connect
82	N.C			No Connect
83	GND			
84	TX0p	I	HS I/O	Lane 0 Transmitter Input (Positive)
85	TX0n	I	HS I/O	Lane 0 Transmitter Input (Negative)
86	GND			
87	TX1p	I	HS I/O	Lane 1 Transmitter Input (Positive)
88	TX1n	I	HS I/O	Lane 1 Transmitter Input (Negative)
89	GND			
90	N.C			No Connect

91	N.C			No Connect
92	GND			
93	N.C			No Connect
94	N.C			No Connect
95	GND			
96	TX2p	I	HS I/O	Lane 2 Transmitter Input (Positive)
97	TX2n	I	HS I/O	Lane 2 Transmitter Input (Negative)
98	GND			
99	TX3p	I	HS I/O	Lane 3 Transmitter Input (Positive)
100	TX3n	I	HS I/O	Lane 3 Transmitter Input (Negative)
101	GND			
102	N.C			No Connect
103	N.C			No Connect
104	GND			

IX. 100Gb/s CFP Mechanical Specifications

100Gb/s CFP2 mechanical dimensions should be compliant with CFP2 MSA specification.

Detailed dimensions are shown in Figure 10.

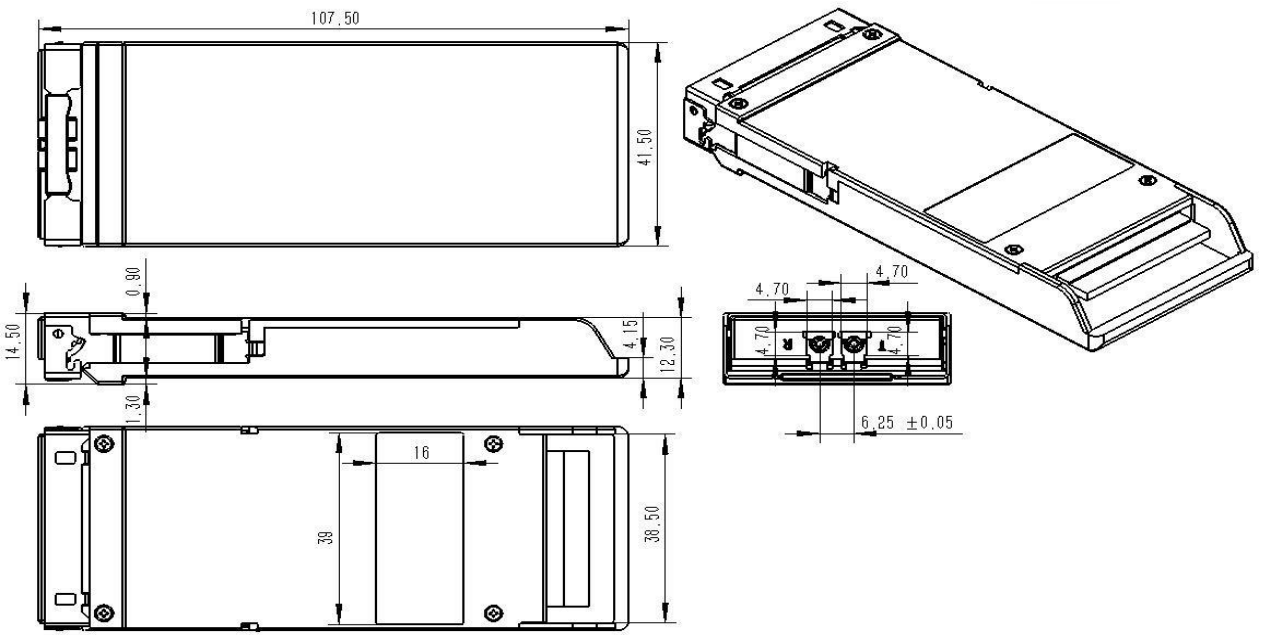


Figure 10 - 100Gb/s CFP2 Mechanical Dimensions(unit:mm)

X. Management Interface

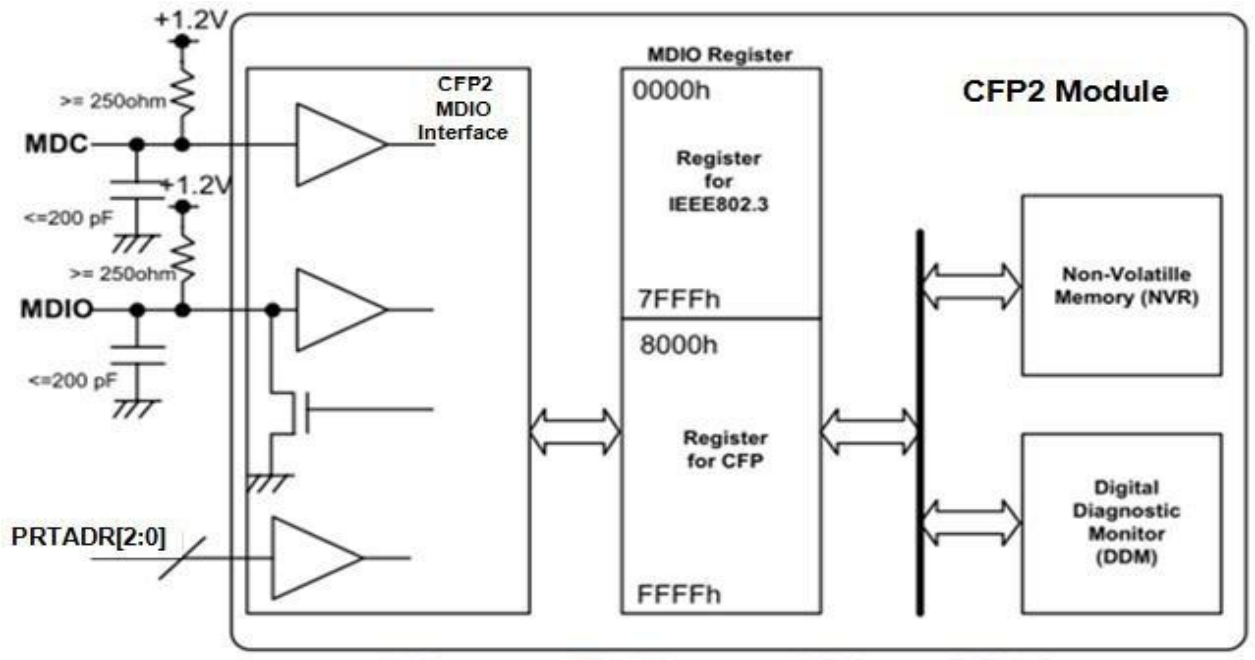


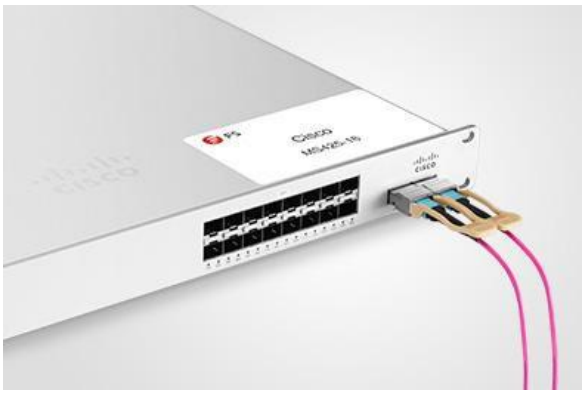
Figure 12 - CFP MDIO Interface

Test Center

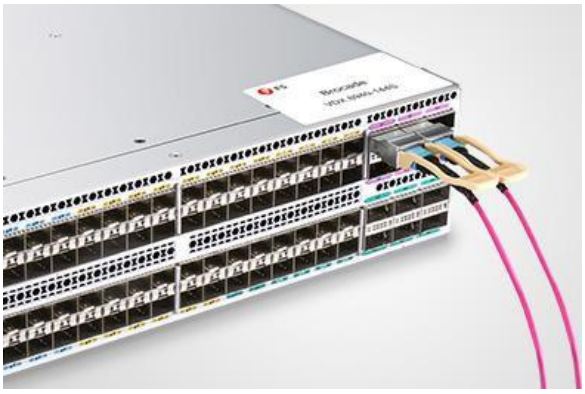
I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.

Cisco Catalyst C9500-24Y4C



Cisco MS425-16



Brocade VDX 6940-144S

Dell EMC Networking Z9100-ON

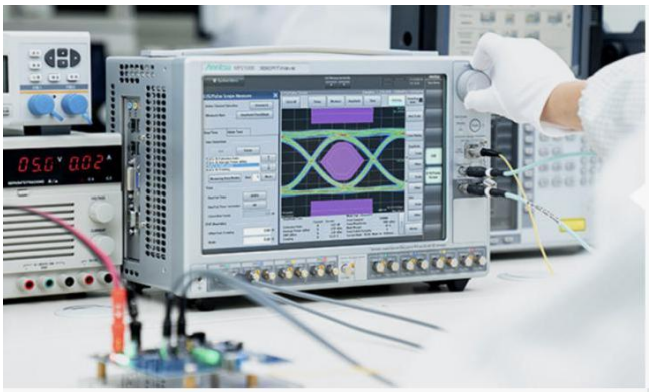
Force⑩tm S60-44T

HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Single Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator the input and output signal quality.

- Eye Pattern Measurements: Jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0℃ to 70℃
- Extended: -5℃ to 85℃
- Industrial: -40℃ to 85℃

3. Transfer Rate and Protocol Testing

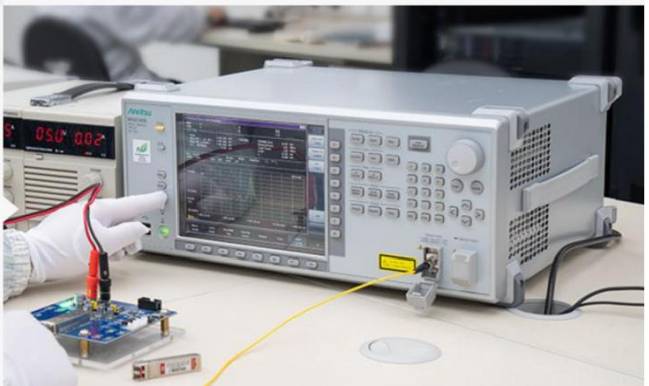
Test the actual transfer data rate and the transmission ability under different protocols with Networks Master Pro.

- Ethernet
- Fiber Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

Part Number	Description
CFP-SR10-100G	CFP 100GBASE-SR10 850nm 150m Transceiver Module
CFP-LR4-100G	CFP 100GBASE-LR4 1310nm 10km Transceiver Module
CFP-ER4-100G	CFP 100GBASE-ER4 1310nm 40km Transceiver Module
CFP2-LR4-100G	CFP2 100GBASE-LR4 1310nm 10km Transceiver Module
CFP4-LR4-100G	CFP4 100GBASE-LR4 1310nm 10km Transceiver Module
CXP-SR10-100G	CXP 100GBASE-SR10 850nm 150m Transceiver Module

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