

# 400GBASE-ER8 QSFP-DD PAM4 1310nm 40km LC SMF DOM Optical Transceiver Module

QSFPDD-ER8-400G



## Application

- 400GBASE-ER8 400G Ethernet
- Data Center
- Telecom
- 40km Transmission on Single Mode Fiber

## Features

- Compliant with IEEE std 802.3cnTM-2019:
  - 400GBASE-ER8 optical interface
  - 400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 5.0 with duplex LC connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Two wire serial Interface with digital diagnostic monitoring
- Class 1/1M Laser
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Operating case temperature: 0°C to 70°C

## Product Specifications

### I. Absolute Maximum Ratings

It has to be noted that the operation in of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Max.	Unit	Notes
<b>Storage Temperature</b>	T <sub>S</sub>	-40	85	°C	
<b>Supply Voltage</b>	V <sub>CC</sub>	-0.5	3.6	V	
<b>Relative Humidity (non-condensing)</b>	RH	5	95	%	
<b>Data Input Voltage Differential</b>	I <sub>V</sub> DIP-V <sub>DIN</sub> I	-	1	V	
<b>Control Input Voltage</b>	V <sub>I</sub>	-0.3	V <sub>CC</sub> +0.5	V	
<b>Control Output Current</b>	I <sub>O</sub>	-20	20	mA	

### II. Recommended Operating Environment

Electrical and optical characteristics below are defined under this operating environment, un- less otherwise specified.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Operating Case Temperature</b>	T <sub>OPR</sub>	0	-	70	°C	
<b>Power Supply Voltage</b>	V <sub>CC</sub>	3.135	3.3	3.465	V	
<b>Instantaneous peak current at hot plug</b>	I <sub>CC_IP</sub>	-	-	5600	mA	
<b>Sustained peak current at hot plug</b>	I <sub>CC_SP</sub>	-	-	4620	mA	
<b>Maximum Power Dissipation</b>	P <sub>D</sub>	-	-	14	W	
<b>Maximum Power Dissipation, Low Power Mode</b>	P <sub>DLP</sub>	-	-	1.5	W	
<b>Signalling Speed per Lane</b>	DRL	-	26.5625	-	GBd	
<b>Control Input Voltage High</b>	V <sub>IH</sub>	V <sub>CC</sub> *0.7	-	V <sub>CC</sub> +0.3	V	
<b>Control Input Voltage Low</b>	V <sub>IL</sub>	-0.3	-	V <sub>CC</sub> *0.3	V	
<b>Two Wire Serial Interface Clock Rate</b>	-	-	-	400	kHz	
<b>Power Supply Noise</b>	-	-	-	66	mVpp	
<b>Rx Differential Data Output Load</b>	-	-	100	-	Ohm	
<b>Operating Distance</b>	-	0.002	-	40	km	1

Note 1: Channel insertion loss is 18dB for 40km.

### III. Functional Characteristics (Optical)

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Transmitter</b>						
<b>Wavelength L0</b>	$\lambda_{C0}$	1272.55	1273.55	1274.54	nm	
<b>Wavelength L1</b>	$\lambda_{C1}$	1276.89	1277.89	1278.89	nm	
<b>Wavelength L2</b>	$\lambda_{C2}$	1281.25	1282.26	1283.27	nm	
<b>Wavelength L3</b>	$\lambda_{C3}$	1285.65	1286.67	1287.68	nm	
<b>Wavelength L4</b>	$\lambda_{C4}$	1294.53	1295.56	1296.59	nm	
<b>Wavelength L5</b>	$\lambda_{C5}$	1299.02	1300.06	1301.09	nm	
<b>Wavelength L6</b>	$\lambda_{C6}$	1303.54	1304.59	1305.63	nm	
<b>Wavelength L7</b>	$\lambda_{C7}$	1308.09	1309.14	1310.19	nm	
<b>Side Mode Suppression Ratio</b>	SMSR	30	-	-	dB	
<b>Total Average Launch Power</b>	AOP <sub>T</sub>	-	-	14.6	dBm	
<b>Average Launch Power, each lane</b>	AOP <sub>L</sub>	-0.6	-	5.6	dBm	1
<b>Outer Optical Modulation Amplitude (OMA<sub>outer</sub>),each Lane</b>	T <sub>OMA</sub>	2.4	-	6.4	dBm	
<b>Difference in Launch Power between any two Lanes(OMA<sub>outer</sub>)</b>	DT <sub>OMA</sub>	-	-	4	dB	
<b>Launch Power in OMA<sub>outer</sub> minus TDECQ,each lane</b>	T <sub>OMA-TDECQ</sub>	1	-	-	dBm	
<b>Transmitter and Dispersion Eye Closure for PAM4(TDECQ), each lane</b>	TDECQ	-	-	3.4	dB	
<b>TDECQ -10log<sub>10</sub>(Ceq)</b>	-	-	-	3.4	dB	
<b>Average Launch Power of OFF Transmitter,each lane</b>	T <sub>OFF</sub>	-	-	-30	dBm	
<b>Extinction Ratio</b>	ER	6	-	-	dB	
<b>RIN15OMA</b>	RIN	-	-	-132	dB/Hz	
<b>Optical Return Loss Tolerance</b>	ORL	-	-	15	dB	
<b>Transmitter Reflectance</b>	T <sub>R</sub>	-	-	-26	dB	2

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength

Note 2: Transmitter reflectance is defined looking into the transmitter

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Receiver</b>						
<b>Wavelength L0</b>	$\lambda_{C0}$	1272.55	1273.55	1274.54	nm	
<b>Wavelength L1</b>	$\lambda_{C1}$	1276.89	1277.89	1278.89	nm	
<b>Wavelength L2</b>	$\lambda_{C2}$	1281.25	1282.26	1283.27	nm	
<b>Wavelength L3</b>	$\lambda_{C3}$	1285.65	1286.67	1287.68	nm	
<b>Wavelength L4</b>	$\lambda_{C4}$	1294.53	1295.56	1296.59	nm	
<b>Wavelength L5</b>	$\lambda_{C5}$	1299.02	1300.06	1301.09	nm	
<b>Wavelength L6</b>	$\lambda_{C6}$	1303.54	1304.59	1305.63	nm	
<b>Wavelength L7</b>	$\lambda_{C7}$	1308.09	1309.14	1310.19	nm	
<b>Damage Threshold, each Lane</b>	AOP <sub>D</sub>	-3.4	-	-	dBm	
<b>Average Receive Power, each Lane</b>	AOP <sub>R</sub>	-18.6	-	-4.4	dBm	
<b>Receive Power (OMA<sub>outer</sub>), each Lane</b>	OMA <sub>R</sub>	-	-	-3.6	dBm	
<b>Difference in Receive Power between any two Lanes (OMA<sub>outer</sub>)</b>	DR <sub>OMA</sub>	-	-	5.8	dB	
<b>Receiver Reflectance</b>	RR	-	-	-26	dB	
<b>Receiver Sensitivity (OMA<sub>outer</sub>), each Lane</b>	S <sub>OMA</sub>	-	-	Max(-16.1, SECQ - 17.5)	dBm	1
<b>Stressed Receiver Sensitivity (OMA<sub>outer</sub>), each Lane</b>	SRS	-	-	-14.1	dBm	2
<b>Conditions of stressed receiver sensitivity test:</b>						
<b>Stressed eye closure for PAM4 (SECQ), lane under test</b>	-	-	3.4	-	dB	
<b>SECQ - 10log<sub>10</sub>(C<sub>eq</sub>), lane under test</b>	-	-	-	3.4	dB	
<b>OMA<sub>outer</sub> of each aggressor lane</b>	-	-	-8.3	-	dBm	
<b>Stressed eye closure for PAM4 (SECQ), lane under test</b>	-	-	3.4	-	dB	

Note 1: Receiver sensitivity (OMA<sub>outer</sub>), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.

Note 2: Measured with conformance test signal at TP3 for the BER = 2.4x10<sup>-4</sup>

## IV. Electrical Characteristics

Electrical Specification High Speed Signal (compliant with IEEE 802.3 400GAUI-8)

### Receiver (Module Output)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>AC common-mode output Voltage (RMS)</b>		-	-	17.5	mV	
<b>Differential output Voltage</b>		-	-	900	mV	
<b>Near-end Eye height, differential</b>		70	-	-	mV	
<b>Far-end Eye height, differential</b>		30	-	-	mV	
<b>Far end pre-cursor ratio</b>		-	-	2.5	%	
<b>Differential Termination Mismatch</b>		-	-	10	%	
<b>Transition Time (min, 20% to 80%)</b>		9.5	-	-	ps	
<b>DC common mode Voltage</b>		-350	-	2850	mV	

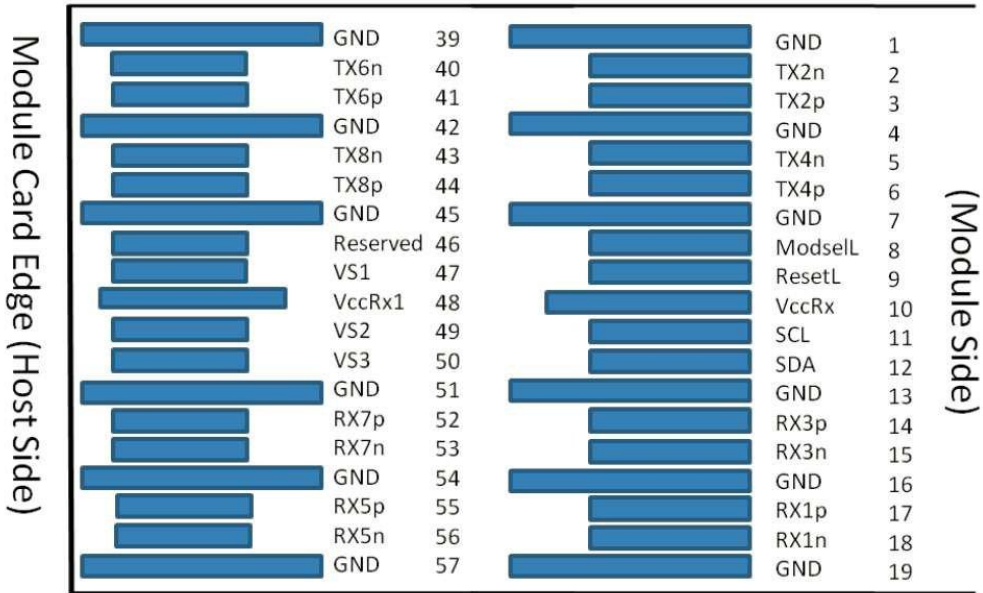
### Transmitter (Module Input)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Differential pk-pk input Voltage tolerance</b>		900	-	-	mV	
<b>Differential termination mismatch</b>		-	-	10	%	
<b>Single-ended voltage tolerance range</b>		-0.4	-	3.3	V	
<b>DC common mode Voltage</b>		-350	-	2850	mV	

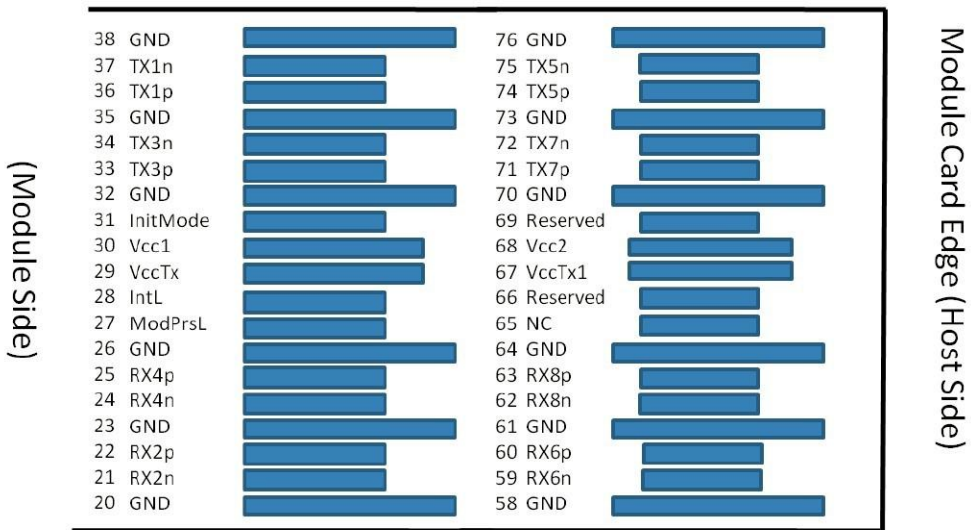
Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 5.1)

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Module output SCL and SDA</b>	V <sub>OL</sub>	0	0.4	V	
<b>Module Input SCL and SDA</b>	V <sub>IL</sub>	-0.3	V <sub>CC</sub> *0.3	V	
	V <sub>IH</sub>	V <sub>CC</sub> *0.7	V <sub>CC</sub> +0.5	V	
<b>InitMode, ResetL and ModSelL</b>	V <sub>IL</sub>	-0.3	0.8	V	
	V <sub>IH</sub>	2	V <sub>CC</sub> +0.3	V	
<b>IntL</b>	V <sub>OL</sub>	0	0.4	V	
	V <sub>OH</sub>	V <sub>CC</sub> -0.5	V <sub>CC</sub> +0.3	V	

### V. Pin Assignment



Bottom side viewed from bottom



Top side viewed from top

Pin definitions of the module high speed inputs/outputs

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

## VI. Timing for Soft Control and Status Functions

Parameter	Symbol	Min.	Max.	Unit	Notes
<b>MgmtInit Duration</b>		-	2000	ms	
<b>ResetL Assert Time</b>	t_reset_init	10	-	μs	
<b>IntL Assert Time</b>	ton_IntL	-	200	ms	
<b>IntL Deassert Time</b>	toff_IntL	-	500	μs	
<b>Rx LOS Assert Time</b>	ton_losf	-	100	ms	
<b>Flag Assert Time</b>	ton_flag	-	200	ms	
<b>Mask Assert Time</b>	ton_mask	-	100	ms	
<b>Mask Deassert Time</b>	toff_mask	-	100	ms	
<b>Module Select Wait Time</b>	ModSelL Wait Time	-	N/A		Not support

## VII. Timing for Squelch and Disable

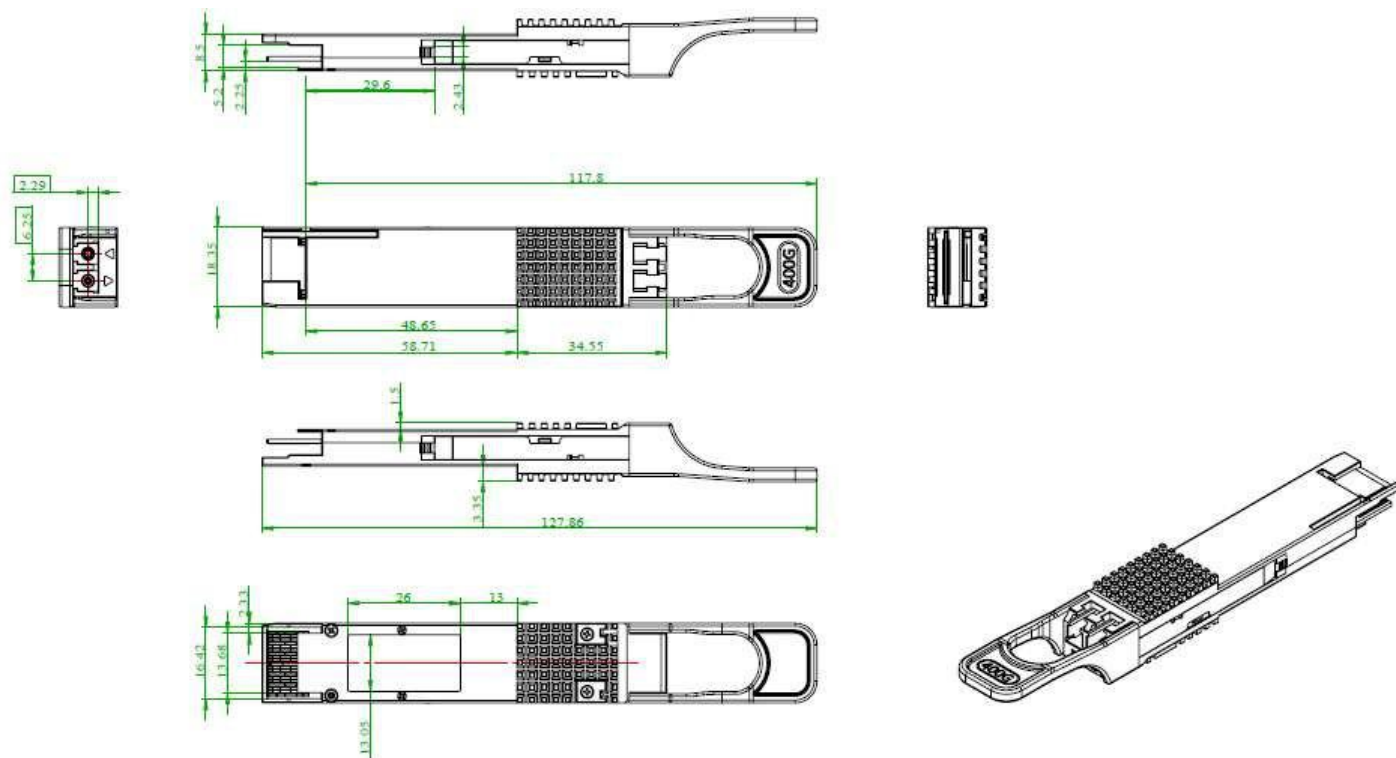
Parameter	Symbol	Min.	Max.	Unit	Notes
<b>Rx Squelch Assert Time</b>	ton_Rxsq	-	50	ms	
<b>Tx Squelch Assert Time</b>	ton_Txsq	-	400	ms	
<b>Tx Squelch Deassert Time</b>	toff_Txsq	-	1500	ms	Based on modulation
<b>Tx Disable Assert Time (fast mode)</b>	ton_Txdisf	-	3	ms	
<b>Tx Disable Deassert Time (fast mode)</b>	toff_Txdisf	-	10	ms	
<b>Rx Output Disable Assert Time</b>	ton_Rxdis	-	100	ms	
<b>Rx Output Disable Deassert Time</b>	toff_Rxdis	-	100	ms	
<b>Squelch Disable Assert Time</b>	ton_sqdis	-	N/A	ms	Not support
<b>Squelch Disable Deassert Time</b>	toff_sqdis	-	N/A	ms	Not support



## VIII. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	$\pm 3$	$^{\circ}\text{C}$	Internal
Voltage	0 to $V_{\text{CC}}$	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-0.6 to +5.6	$\pm 3$	dB	Internal
Rx Receive Power (Each Lane)	-18.6 to -4.4	$\pm 3$	dB	Internal

### IX. Diagram Mechanical Drawing



## Test Center

FS.COM transceivers are tested to ensure connectivity and compatibility in our test center before shipped out. FS.COM test center is supported by a variety of mainstream original brand switches and groups of professional staff, helping our customers make the most efficient use of our products in their systems, network designs and deployments.

The original switches could be found nowhere but at FS.COM test center, eg: Juniper MX960 & EX 4300 series, Cisco Nexus 9396PX & Cisco ASR 9000 Series, HP 5900 Series & HP 5406R ZL2 V3(J9996A), Arista 7050S-64, Brocade ICX7750-26Q & ICX6610-48, Avaya VSP 7000 MDA 2, etc.



Cisco ASR 9000 Series(A9K-MPA-1X40GE)



ARISTA 7050S-64(DCS-7050S-64)



Juniper MX960



Brocade ICX 7750-26Q



Extreme Networks X670V VIM-40G4X



Mellanox M3601Q



Dell N4032F



HP 5406R ZL2 V3(J9996A)



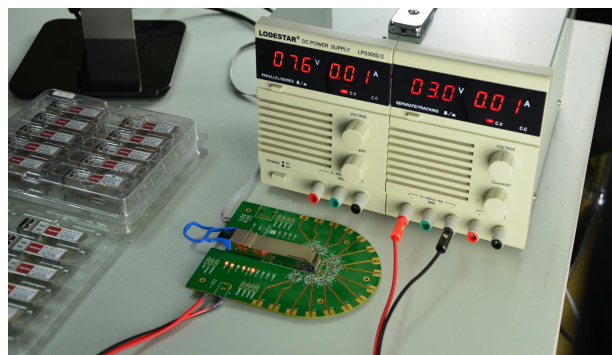
AVAYA 7024XLS(7002QQ-MDA)

## Test Assured Program

FS.COM truly understands the value of compatibility and interoperability to each optics. Every module FS.COM provides must run through programming and an extensive series of platform diagnostic tests to prove its performance and compatibility. In our test center, we care of every detail from staff to facilities—professionally trained staff, advanced test facilities and comprehensive original-brand switches, to ensure our customers to receive the optics with superior quality.



Our smart data system allows effective product management and quality control according to the unique serial number, properly tracing the order, shipment and every part.



Our in-house coding facility programs all of our parts to standard OEM specs for compatibility on all major vendors and systems such as Cisco, Juniper, Brocade, HP, Dell, Arista and so on.



With a comprehensive line of original-brand switches, we can recreate an environment and test each optics in practical application to ensure quality and distance.



The last test assured step to ensure our products to be shipped with perfect package.

## Order Information

Part Number	Description
QSFPDD-SR8-400G	QSFP-DD 400GBASE-SR8 850nm 100m Transceiver
QSFPDD-DR4-400G	QSFP-DD 400GBASE-DR4 1310nm 500m Transceiver
QDD-DR4-400G-Si	QSFP-DD 400GBASE-DR4 1310nm 500m Silicon Photonics Transceiver
QSFPDD-XDR4-400G	QSFP-DD 400GBASE-DR4+ 1310nm 2km Transceiver
QSFPDD-FR4-400G	QSFP-DD 400GBASE-FR4 1310nm 2km Transceiver
QSFPDD-LR4-400G	QSFP-DD 400GBASE-LR4 1310nm 10km Transceiver
QSFPDD-LR8-400G	QSFP-DD 400GBASE-LR8 1310nm 10km Transceiver
QSFPDD-ER8-400G	QSFP-DD 400GBASE-ER8 QSFP-DD PAM4 1310nm 40km Transceiver



 <https://www.fs.com>



The information in this document is subject to change without notice. FS has made all efforts to ensure the accuracy of the information, but all information in this document does not constitute any kind of warranty.