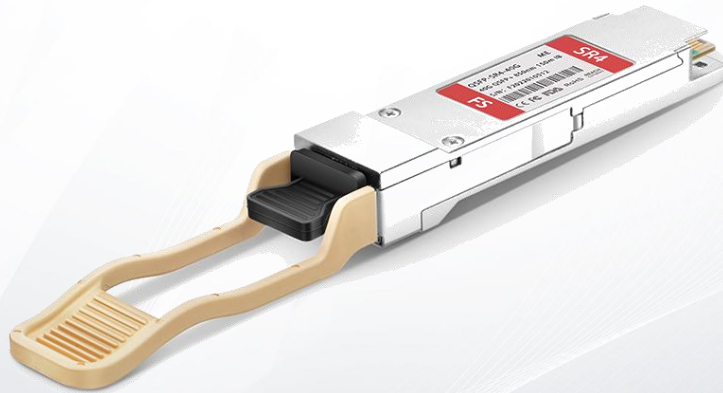


40GBASE-SR4 QSFP+ 850nm 150m DOM Transceiver for InfiniBand FDR10

QSFP-SR4-40G



Application

- InfiniBand FDR10

Standards

- IEEE 802.3 40GBASE-SR4
- QSFP+ MSA
- SFF-8436
- SFF-8472

Features

- Maximum Data Rate per Lane: 10.3125Gb/s
- Max. Power Consumption 1.5W
- Maximum Link Length of 100m on OM3 MMF or 150m on OM4 MMF
- 3.3V Supply Voltage
- 0~70 °C Case Operating Temperature
- 850nm 4 VCSEL Lasers and 4 Channels PIN Photo Detectors
- MTP/MPO-12 Receptacle
- 2-Wire Interface for Management and Digital Diagnostic Monitoring
- Class 1 Laser Safety

Description

The QSFP+ Optical Transceiver Module is designed for use in 40Gb/s FDR10 InfiniBand systems throughput up to 150m over OM4 or 100m over OM3 multimode fiber (MMF) using a wavelength of 850nm via a MTP/MPO-12 connector. This transceiver is compliant with QSFP+ MSA, SFF-8436, SFF-8472 and IEEE 802.3ba standards. Digital diagnostics functions are also available via the I2C interface, as specified by the QSFP+ MSA, to allow access to real-time operating parameters.

With these features, this easy to install, hot swappable transceiver is suitable to be used in various applications, such as InfiniBand, data centers, high-performance computing networks, enterprise core and distribution layer applications.

Product Specifications

I. Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typical | Max. | Unit |
|---|----------|------|---------|--------------|------|
| Storage Temperature | T_S | -40 | | 85 | °C |
| Supply Voltage | V_{CC} | -0.5 | | 3.6 | V |
| Relative Humidity (Non-condensing) | RH | 5 | | 95 | % |
| Input Voltage | V_{in} | -0.5 | | $V_{CC}+0.5$ | V |

II. Recommended Operating Conditions

| Parameter | Symbol | Min. | Typical | Max. | Unit |
|-----------------------------------|-----------|-------|---------|-------|------|
| Operating Case Temperature | T_{OPR} | 0 | | 70 | °C |
| Power Supply Voltage | V_{CC} | 3.135 | 3.3 | 3.465 | V |
| Power Supply Current | I_{CC} | | | 475 | mA |
| Maximum Power Dissipation | P_D | | | 1.5 | W |
| Data Rate per Lane | DR | | 10.3125 | | Gb/s |

| Parameter | Symbol | Min. | Typical | Max. | Units | Notes |
|------------------------------|--------|------|---------|------|-------|-------|
| Operating Distance (MMF OM3) | | 0.5 | | 100 | m | |
| Operating Distance (MMF OM4) | | 0.5 | | 150 | m | |

III. Optical Characteristics

| Parameter | Symbol | Min. | Typical | Max. | Units |
|-----------|--------|------|---------|------|-------|
|-----------|--------|------|---------|------|-------|

Transmitter

| | | | | | |
|--|-----------------|------|---------|------|------|
| Mean Wavelength, each Lane | λ | 840 | 850 | 860 | nm |
| Data Rate per Lane | DR | | 10.3125 | | Gbps |
| Spectral Width (RMS) | $\Delta\lambda$ | | | 0.65 | nm |
| Optical Power, each Lane | P_{OUT} | -7.6 | | 2.4 | dBm |
| OMA per Lane | P_{oma} | -5.6 | | 3 | dBm |
| Peak Power, each Lane | P_{peak} | | | 4 | dBm |
| Extinction Ratio | ER | 3 | | | dB |
| TDP, each Lane | TDP | | | 3.5 | dB |
| Optical Return Loss Tolerance | | | | 12 | dB |
| Average Launch Power Tx_Off, each Lane | | | | -30 | dBm |

Receiver

| | | | | | |
|-----------------------|-----------|-----|-----|-----|----|
| Wavelength, each Lane | λ | 840 | 850 | 860 | nm |
|-----------------------|-----------|-----|-----|-----|----|

| Parameter | Symbol | Min. | Typical | Max. | Units |
|---|---------|------|---------|------|-------|
| Data Rate per Lane | DR | | 10.3125 | | Gbps |
| Average Power at Receiver, each Lane | | -9.5 | | 2.4 | dBm |
| Rx OMA per Lane | OMA | | | 3 | dBm |
| Stressed Receiver Sensitivity OMA, each Lane | SRS | | | -5.4 | dBm |
| Peak Power, each Lane | | | | 4 | dBm |
| Receiver Reflectance | RX_R | | | -12 | dB |
| LOS Assert | LOS_A | -30 | | | dBm |
| LOS De-assert | LOS_D | | | -10 | dBm |
| LOS Hysteresis | | 0.5 | | | dB |

Note:

1. Measured with a PRBS2³¹-1 test pattern @10.3125Gbps, BER≤10⁻¹².

IV. Electrical Characteristics

1. High Speed Electrical Specifications

| Parameter | Symbol | Min. | Typical | Max. | Units |
|--------------------------------|---------------|--------------|---------|----------|----------|
| Supply Voltage | V_{CC} | 3.135 | | 3.465 | V |
| Supply Current | I_{CC} | | | 450 | mA |
| Input Differential Impedance | | 90 | 100 | 110 | Ω |
| Differential Data Input Swing | $V_{IN,P-P}$ | 300 | | 1100 | mVpp |
| Differential Data Output Swing | $V_{OUT,P-P}$ | 300 | | 850 | mVpp |
| Input Logic Level High | | 2 | | V_{CC} | |
| Input Logic Level Low | | 0 | | 0.8 | |
| Output Logic Level High | | $V_{CC}-0.5$ | | V_{CC} | |
| Output Logic Level Low | | 0 | | 0.4 | |

2. 2-Wire Electrical Specifications

| Parameter | Symbol | Min. | Max. | Units |
|---|--------------------|------------------------|------------------------|-------|
| Host 2-Wire V_{CC} Voltage | $V_{CC_Host_2w}$ | 3.14 | 3.46 | V |
| SCL and SDA Voltage | V_{OL} | 0 | 0.4 | V |
| | V_{OH} | $V_{CC_Host_2w}-0.5$ | $V_{CC_Host_2w}+0.3$ | V |
| | V_{IL} | -0.3 | $V_{CC}T*0.3$ | V |
| | V_{IH} | $V_{CC}T*0.7$ | $V_{CC}T+0.5$ | V |
| Input Current on the SCL and SDA Contacts | I_i | -10 | 10 | mA |

V. Timing

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|--|-----------|------|------|------|-------|
| Clock Frequency | f_scl | 100 | 400 | kHZ | 1 |
| Clock Pulse Width Low | t_low | 1.3 | | μs | |
| Clock Pulse Width High | t_high | 0.6 | | μs | |
| Time Bus Free Before New Transmission Can Start | t_buf | 20 | | μs | 2 |
| START Hold Time | t_HD, STA | 0.6 | 0 | μs | |
| START Set-up Time | t_SU, STA | 0.6 | | μs | |
| Data In Hold Time | t_HD, DAT | 0 | | μs | |
| Data In Set-up Time | t_SU, DAT | 0.1 | | μs | |
| Input Rise Time (100kHz) | tr, 100 | | 1000 | ns | 3 |
| Input Rise Time (400kHz) | tr, 100 | | 300 | ns | 3 |
| Input Fall Time (100kHz) | tf, 100 | | 300 | ns | 4 |
| Input Fall Time (400kHz) | tf, 400 | | 300 | ns | 4 |
| STOP Set-up Time | t_SU, STO | 0.6 | | us | |

Notes:

- Module shall operate with fSCL up to 100 kHz without requiring clock stretching. The module may clock stretch with fSCL greater than 100 kHz and up to 400 kHz.
- Between STOP and START and between ACK and ReSTART.
- From (VIL, MAX-0.15) to (VIH, MIN+0.15).
- From (VIH, MIN+0.15) to (VIL, MAX-0.15).

VI. Pin Definitions



| Pin | Logic | Symbol | Name/Description | Plug Sequence | Notes |
|-----|-------|--------|-------------------------------------|---------------|-------|
| 1 | | GND | Ground | 1 | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3 | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3 | |
| 4 | | GND | Ground | 1 | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3 | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3 | |
| 7 | | GND | Ground | 1 | 1 |

| Pin | Logic | Symbol | Name/Description | Plug Sequence | Notes |
|-----|-------------|--------------------|-----------------------------------|---------------|-------|
| 8 | LVTTTL-I | ModselL | Module Select | 3 | |
| 9 | LVTTTL-I | ResetL | Module Reset | 3 | |
| 10 | | V _{CC} Rx | 3.3V Power Supply Receiver | 2 | 2 |
| 11 | LVC MOS-I/O | SCL | 2-Wire Serial Interface Clock | 3 | |
| 12 | LVC MOS-I/O | SDA | 2-Wire Serial Interface Data | 3 | |
| 13 | | GND | Ground | 1 | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3 | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3 | |
| 16 | | GND | Ground | 1 | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3 | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3 | |
| 19 | | GND | Ground | 1 | 1 |
| 20 | | GND | Ground | 1 | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3 | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3 | |
| 23 | | GND | Ground | 1 | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3 | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3 | |

| Pin | Logic | Symbol | Name/Description | Plug Sequence | Notes |
|-----|---------|--------------------|-------------------------------------|---------------|-------|
| 26 | | GND | Ground | 1 | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3 | |
| 28 | LVTTL-O | IntL | Interrupt | 3 | |
| 29 | | V _{CC} Tx | 3.3V Power Supply Transmitter | 2 | 2 |
| 30 | | V _{CC} 1 | 3.3V Power Supply | 2 | 2 |
| 31 | LVTTL-I | LPMode | Low Power Mode | 3 | |
| 32 | | GND | Ground | 1 | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3 | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3 | |
| 35 | | GND | Ground | 1 | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3 | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3 | |
| 38 | | GND | Ground | 1 | 1 |

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. V_{CC}Rx, V_{CC}1 and V_{CC}Tx are the receiver and transmitter power supplies and shall be applied concurrently. V_{CC}Rx, V_{CC}1 and V_{CC}Tx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500 mA.

VII. Memory Specifications

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|--|--------------|------|------|------|-------|
| Serial Interface Clock Holdoff "Clock Stretching" | T_clock_hold | | 500 | μs | 1 |
| Complete Single or Sequential Write Up to 4 Byte | tWR | | 40 | ms | |
| Complete Sequential Write of 5~8 Byte | tWR | | 80 | ms | |
| Endurance (Write Cycles) | | 10K | | ms | |

Note:

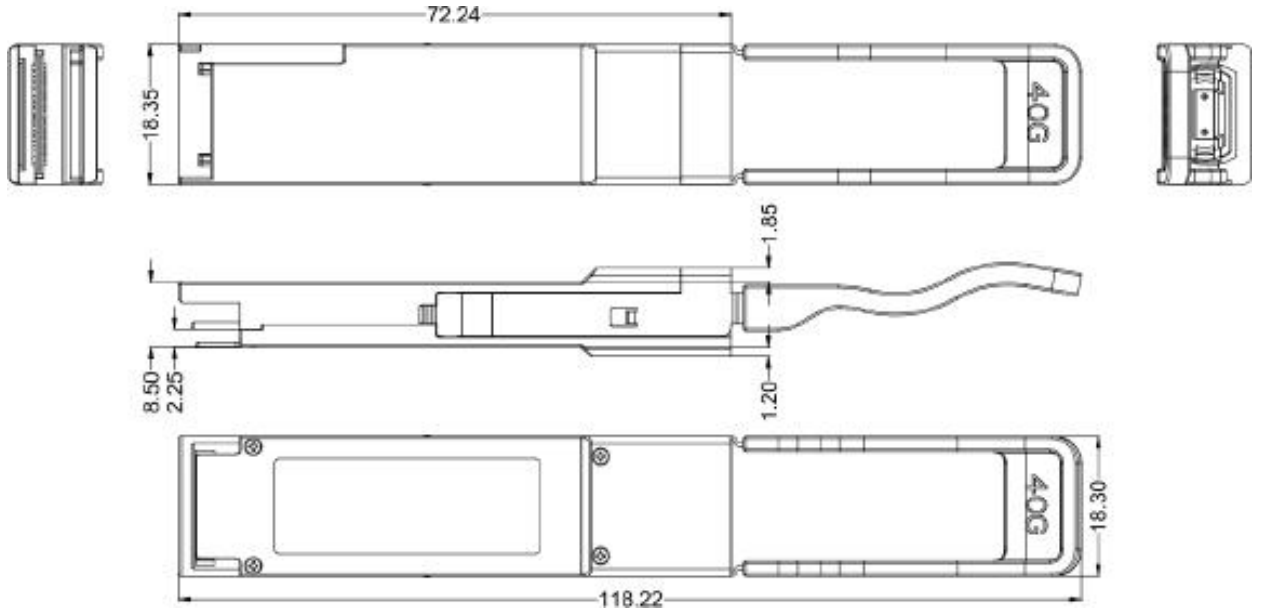
1. Maximum time the QSFP+ module may hold the SCL line low before continuing with a read or write operation.

VIII. Digital Diagnostic Specifications

| Parameter | Range | Accuracy | Unit | Calibration |
|-----------------------------------|-------------------|----------|------|-------------|
| Temperature | 0~70 | ±3 | °C | Internal |
| Voltage | 0~V _{CC} | ±3 | % | Internal |
| Tx Bias Current, each Lane | 0~15 | ±10 | % | Internal |
| Tx Output Power | -7.6~2.4 | ±3 | dB | Internal |
| Rx Power, each Lane | -9.5~2.4 | ±3 | dB | Internal |

IX. Mechanical Specifications

Unit: mm



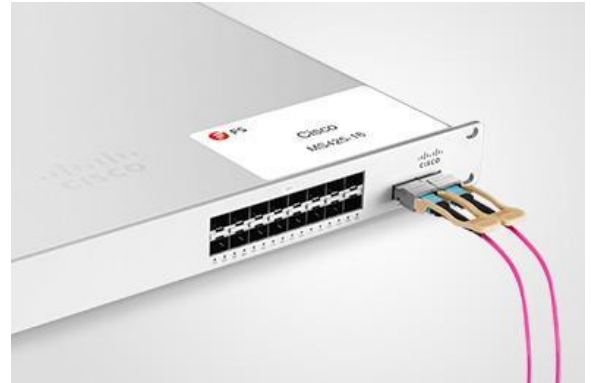
Test Center

I. Compatibility Testing

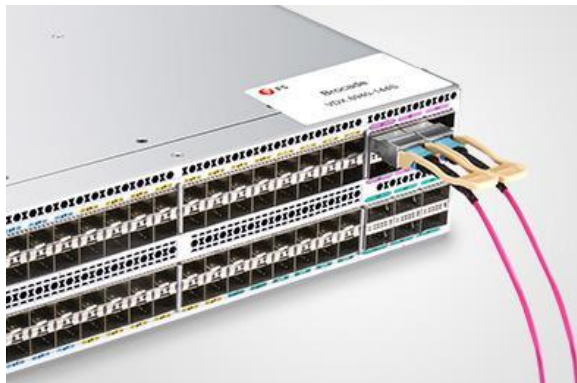
Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.



Cisco Catalyst C9500-24Y4C



Cisco MS425-16



Brocade VDX 6940-144S



Dell EMC Networking Z9100-ON



Force@tm S60-44T



HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in real time as we expand our portfolio.

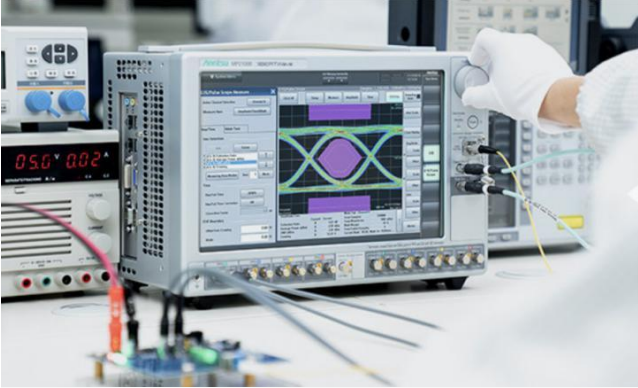
II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.

1. TX/RX Signal Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator to ensure the input and output signal quality.

- Eye Pattern Measurements: jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve



2. Reliability and Stability Testing

Subject the transceivers to dramatic changes in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0 °C to 70 °C
- Extended: -5 °C to 85 °C
- Industrial: -40 °C to 85 °C



3. Transfer Rate and Protocol Testing

Test the actual transfer data rate and the transmission ability under different protocols with Network Master Pro.

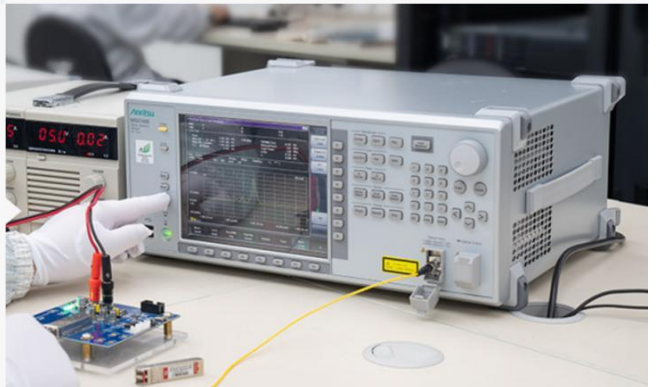
- Ethernet
- Fibre Channel
- SDH/SONET
- CPRI



4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

| Part Number | Description |
|-----------------|--|
| QSFP-SR4-40G | 40GBASE-SR4 QSFP+ 850nm 150m MTP/MPO Transceiver for MMF |
| QSFP-SR4-40G | 40GBASE-SR4 QSFP+ 850nm 150m MTP/MPO Transceiver for MMF, InfiniBand FDR10 |
| QSFP-CSR4-40G | 40GBASE-CSR4 QSFP+ 850nm 400m MTP/MPO Transceiver for MMF |
| QSFP-PIR4-40G | 40GBASE-PLRL4 QSFP+ 1310nm 1.4km MTP/MPO Transceiver for SMF |
| QSFP-LX4-40G | 40GBASE-UNIV QSFP+ 1310nm 2km LC Transceiver for SMF&MMF |
| QSFP-IR4-40G | 40GBASE-LR4L QSFP+ 1310nm 2km LC Transceiver for SMF |
| QSFP-LR4-40G | 40GBASE-LR4 and OTU3 QSFP+ 1310nm 10km LC Transceiver for SMF |
| QSFP-LR4-40G | 40GBASE-LR4 QSFP+ 1310nm 10km LC Transceiver for SMF, InfiniBand FDR10 |
| QSFP-LR4-40G-20 | 40GBASE-LR4 QSFP+ 1310nm 20km LC Transceiver for SMF |
| QSFP-PLR4-40G | 40GBASE-PLR4 QSFP+ 1310nm 10km MTP/MPO Transceiver for SMF |
| QSFP-ER4-40G | 40GBASE-ER4 and OTU3 QSFP+ 1310nm 40km LC Transceiver for SMF |
| QSFP-BD-40G | 40GBASE-SR Bi-Directional QSFP LC Duplex Transceiver for MMF |
| QSFP-BIDI-40G | 40GBASE Bi-Directional QSFP+ 850nm 300m DOM LC Transceiver for MMF |
| QSFP-PLR4-40G-I | 40GBASE-PLR4 QSFP+ PSM4 1310nm 10km Industrial MTP/MPO Transceiver for SMF |



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