800GBASE-PLR8 QSFP-DD 1310nm 10km MTP/MPO-16 SMF Transceiver

QDD800-PLR8-B1

Application

- 800G Ethernet
- Data Center
- Breakout 2x 400G PLR4 or 8x 100G LR

Features

- Typical Power Consumption 18W
- 8x106.25 Gb/s PAM4 Modulation
- Single 3.3V Power Supply
- Operating Case Temperature Range: 0 ~ 70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser Safety

Standards

- Compliant with IEEE 802.3cu-2021
  -8x100GBASE-LR1 Optical Interface
- Compliant with IEEE P802.3ck D3.0
  -8x100GAUI-1 C2M Electrical Interface
- Compliant with QSFP-DD MSA HW Rev 6.01
  -Type 2A with MPO-16 Connector
- Compliant with CMIS Rev 5.0

Description

FS's 800GBASE-PLR8 QSFP-DD transceiver supports up to 10km link lengths over single-mode fiber (SMF) with MPO-16 connectors. This transceiver is compliant with QSFP-DD MSA HW Rev 6.01, IEEE 802.3cu-2021 and CMIS Rev 5.0 standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Data Center, Breakout 2x 400G PLR4 or 8x 100G LR application.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
Data Input Voltage Differential	$\|V_{DIP}-V_{DIN}\|$		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_{OPR}	0		70	°C
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			TBD	mA
Sustained Peak Current at Hot Plug	I_{CC_SP}			TBD	mA

Parameter	Symbol	Min.	Typical	Max.	Unit
Power Dissipation	P_D		18		W
Maximum Power Dissipation, Low Power Mode	P_{DLP}			TBD	W
Signalling Speed per Lane	DRL		53.125		GBd
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V
Two Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise 1 kHz -1 MHz (p-p)				66	mVpp
Operating Distance		2		10000	m

III. Optical Characteristics

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	AOP_L	-1.9		4.8	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane for TDECQ<1.4dB for 1.4dB<=TDECQ<=3.4dB	OMA_{outer}	1.1 –0.3+TDECQ		5	dBm	
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), each Lane	TDECQ			3.4	dB	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter Eye Closure for PAM4 (TECQ), each Lane	TECQ			3.4	dB	
|TDECQ-TECQ|				2.5	dB	
Over/Under-shoot				22	%	
Transmitter Power Excursion				2.8	dBm	
Average Launch Power of OFF Transmitter, each Lane	T_{OFF}			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time	Tr			17	ps	
$RIN_{15.6}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.6	dB	
Transmitter Reflectance	T_R			-26	dB	2
Receiver						
Wavelength	λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOP_D	5.8			dBm	
Average Receive Power, each Lane	AOP_R	-8.2		4.8	dBm	
Receive Power (OMA_{outer}), each Lane	OMA_R			5	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA_{outer}) for TECQ<1.4dB for 1.4dB<=TECQ<=3.4dB	S_{OMA}			–6.1 –7.5+TECQ	dBm	3

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.1	dBm	4
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4(SECQ), Lane Under Test	SECQ		3.4		dB	

Notes:

1. Average launch power, each lane (Min.) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMA_{outer}), each lane (Max.) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.
4. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$.

IV. Electrical Characteristics

1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

Parameter		Symbol	Min.	Typical	Max.	Unit
Receiver (Module Output, TP4)						
AC Common-mode Output Voltage (RMS)					25	mV
Differential Peak-to-peak Output Voltage	**Short Mode**				600	mV
	Long Mode				845	mV
Eye Height		EH	15			mV
Vertical Eye Closure		VEC			12	dB
Common-mode to Differential-mode Return Loss		RLD_C		802.3ck 120G-1		dB
Effective Return Loss		ERL	8.5			dB

Parameter	Symbol	Min.	Typical	Max.	Unit
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Transmitter (Module Input, TP1)					
Differential Pk-pk Input Voltage Tolerance (TP1a)		750			mV
AC Common-mode RMS Voltage Tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RL_{cd}	802.3ck 120G-2			dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerance Range		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V

2. Electrical Specification Low Speed Control and Sense Signals (Compliant with QSFP-DD HW Rev6.01 Table 14)

Parameter	Symbol	Min.	Max.	Unit
Module Output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V

Parameter	Symbol	Min.	Max.	Unit
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	V_{CC}+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V

V. Pin Description

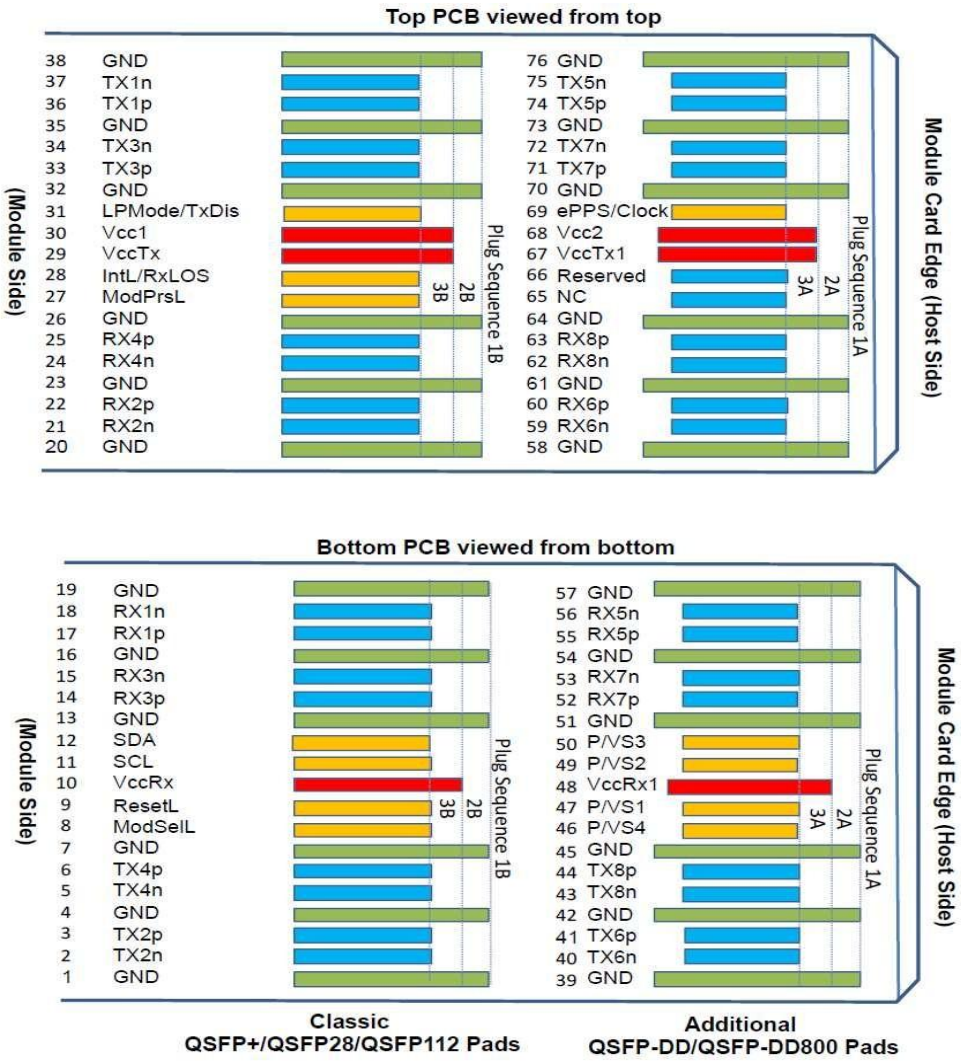


Figure 1 – Pin definitions of the module high speed inputs/outputs

Pin	Symbol	Description	Logic
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	CML-I
3	Tx2p	Transmitter Non-Inverted Data Input	CML-I
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	CML-I
6	Tx4p	Transmitter Non-Inverted Data Input	CML-I
7	GND	Ground	
8	ModSelL	Module Select	LVTTL-I
9	ResetL	Module Reset	LVTTL-I
10	V_{cc}Rx	+3.3V Power Supply Receiver	
11	SCL	TWI Serial Interface Clock	LVCMOS-I/O
12	SDA	TWI Serial Interface Data	LVCMOS-I/O
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	CML-O
15	Rx3n	Receiver Inverted Data Output	CML-O
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	CML-O
18	Rx1n	Receiver Inverted Data Output	CML-O

Pin	Symbol	Description	Logic
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	CML-O
22	Rx2p	Receiver Non-Inverted Data Output	CML-O
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	CML-O
25	Rx4p	Receiver Non-Inverted Data Output	CML-O
26	GND	Ground	
27	ModPrsL	Module Present	LVTTL-O
28	IntL/RxLOS	Interrupt/Optional Rx LOS	LVTTL-O
29	V_{CC}Tx	+3.3V Power Supply Transmitter	
30	V_{CC}1	+3.3V Power Supply	
31	LPMode/TxDis	Low Power Mode/Optional Tx Disable	LVTTL-I
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	CML-I
34	Tx3n	Transmitter Inverted Data Input	CML-I
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	CML-I

Pin	Symbol	Description	Logic
37	Tx1n	Transmitter Inverted Data Input	CML-I
38	GND	Ground	
39	GND	Ground	
40	Tx6n	Transmitter Inverted Data Input	CML-I
41	Tx6p	Transmitter Non-Inverted Data Input	CML-I
42	GND	Ground	
43	Tx8n	Transmitter Inverted Data Input	CML-I
44	Tx8p	Transmitter Non-Inverted Data Input	CML-I
45	GND	Ground	
46	P/VS4	Programmable/Module Vendor Specific 4	LVCMOS/CML-I
47	P/VS1	Programmable/Module Vendor Specific 1	LVCMOS/CML-I
48	V_{CC}Rx1	3.3V Power Supply	
49	P/VS2	Programmable/Module Vendor Specific 2	LVCMOS/CML-O
50	P/VS3	Programmable/Module Vendor Specific 3	LVCMOS/CML-O
51	GND	Ground	
52	Rx7p	Receiver Non-Inverted Data Output	CML-O
53	Rx7n	Receiver Inverted Data Output	CML-O
54	GND	Ground	

Pin	Symbol	Description	Logic
55	Rx5p	Receiver Non-Inverted Data Output	CML-O
56	Rx5n	Receiver Inverted Data Output	CML-O
57	GND	Ground	
58	GND	Ground	
59	Rx6n	Receiver Inverted Data Output	CML-O
60	Rx6p	Receiver Non-Inverted Data Output	CML-O
61	GND	Ground	
62	Rx8n	Receiver Inverted Data Output	CML-O
63	Rx8p	Receiver Non-Inverted Data Output	CML-O
64	GND	Ground	
65	NC	Not Connected	
66	Reserved		
67	V_{CC}Tx1	3.3V Power Supply	
68	V_{CC}2	3.3V Power Supply	
69	EPPS/Clock	1PPS PTP Clock or Reference Clock Input	LVCMOS-I
70	GND	Ground	
71	Tx7p	Transmitter Non-Inverted Data Input	CML-I
72	Tx7n	Transmitter Inverted Data Input	CML-I

Pin	Symbol	Description	Logic
73	GND	Ground	
74	Tx5p	Transmitter Non-Inverted Data Input	CML-I
75	Tx5n	Transmitter Inverted Data Input	CML-I
76	GND	Ground	

VI. Recommended QSFP-DD Host Board Schematic

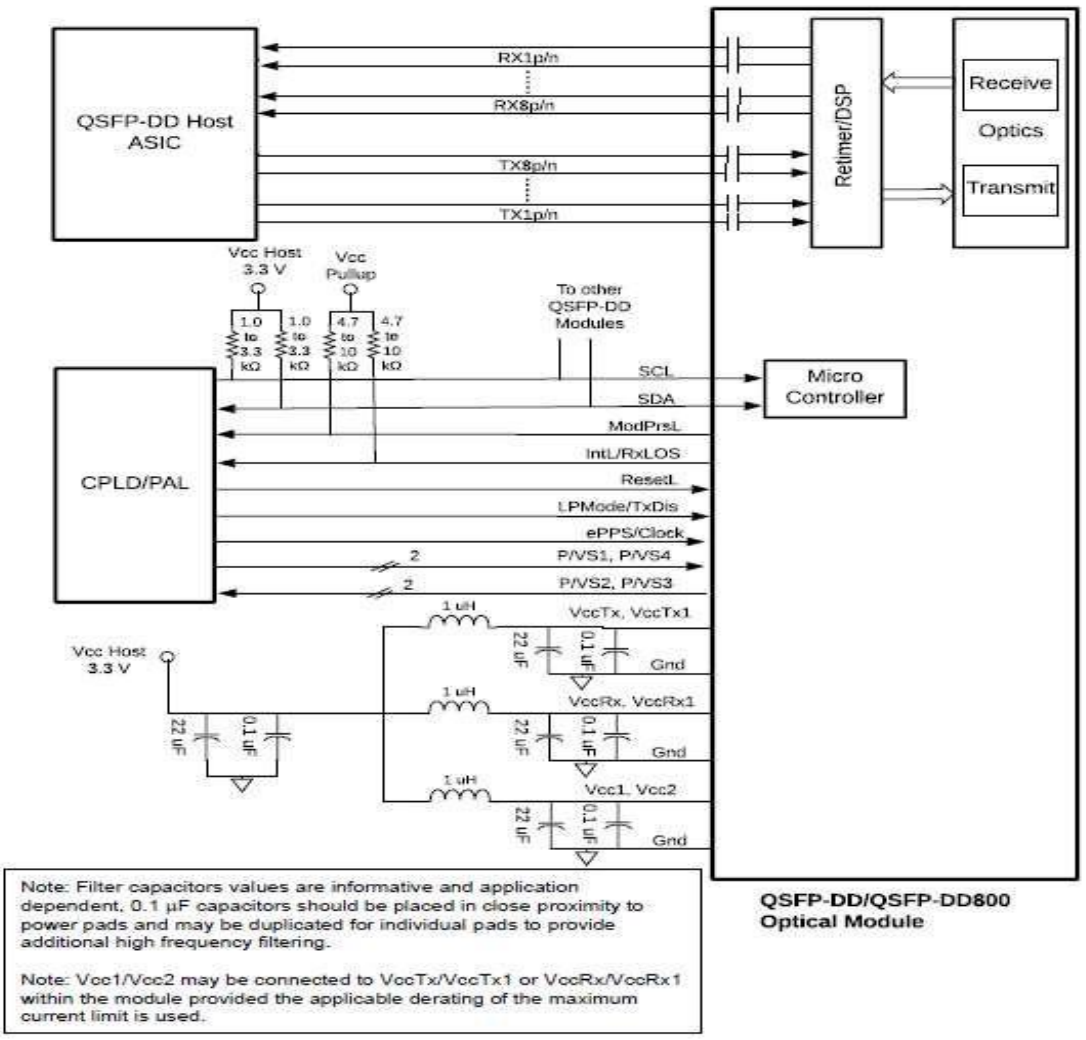
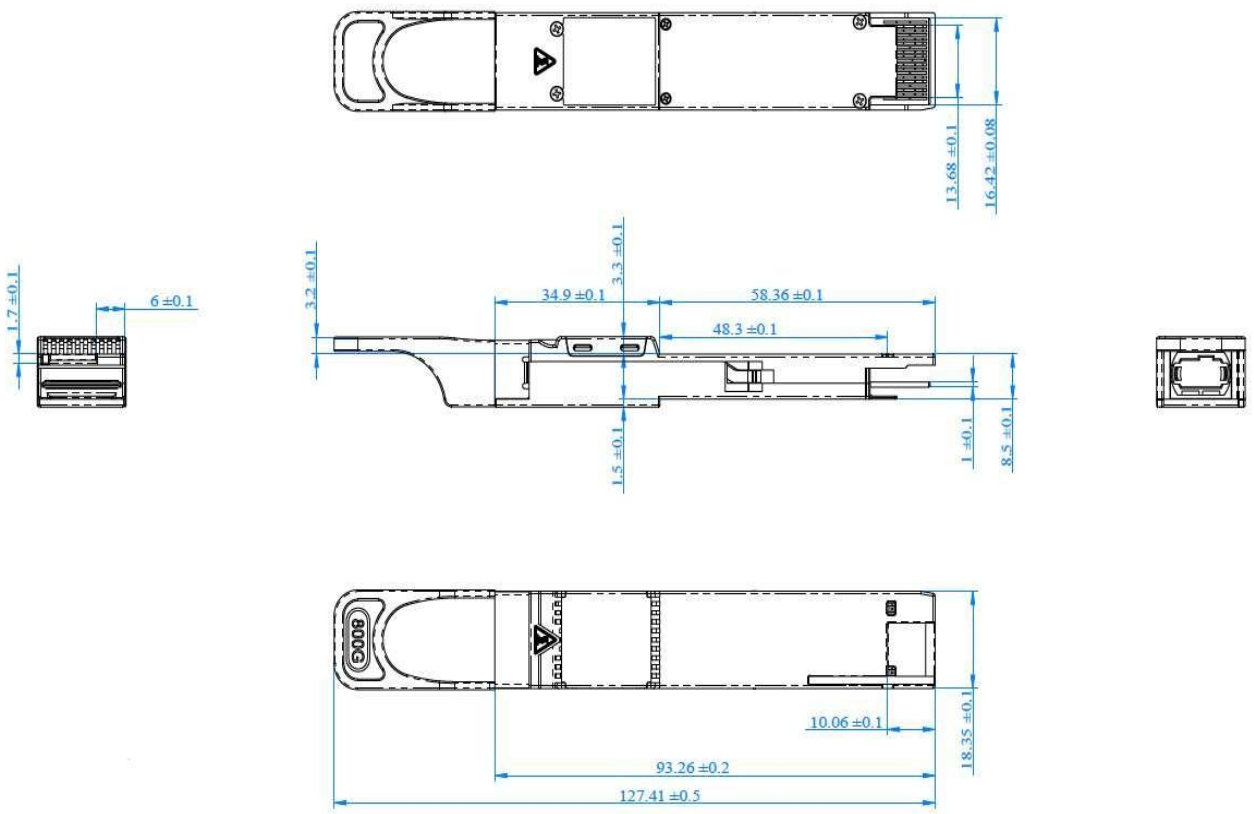


Figure 2 – Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

VII. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (each Lane)	-1.9 to +4.8	±3	dB	Internal
Rx Receive Power (each Lane)	-8.2 to +4.8	±3	dB	Internal

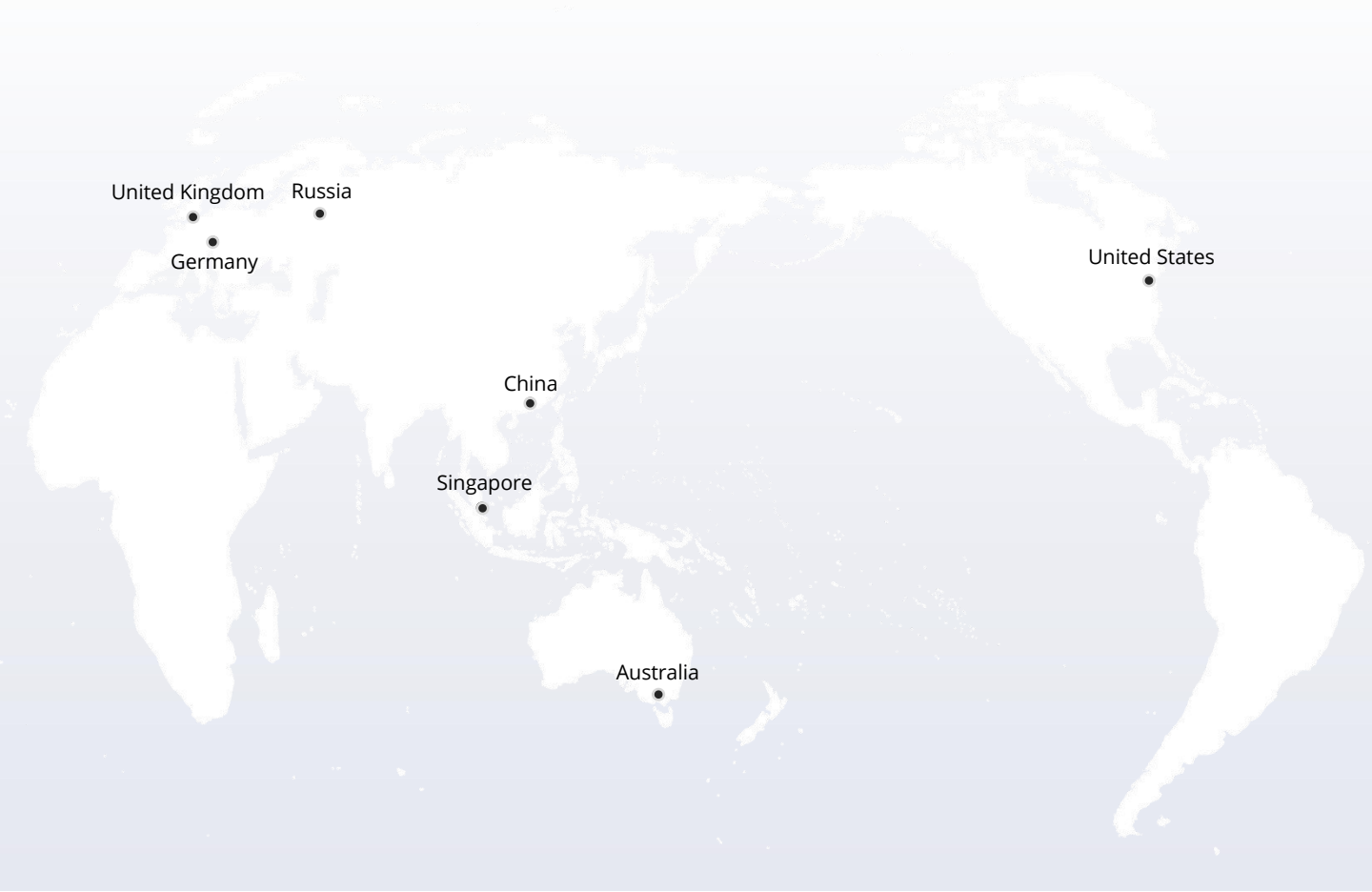
VIII. Diagram Mechanial Drawing



unit: mm

Order Information

Part Number	Description
QDD800-DR8-B1	800GBASE-DR8 QSFP-DD PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver
QDD800-2FR4-C1	800GBASE-2FR4 QSFP-DD PAM4 1310nm 2km DOM Dual CS SMF Optical Transceiver
OSFP800-DR8-B1	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver
OSFP800-DR8-B2	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO SMF Optical Transceiver
OSFP800-XDR8-B1	800GBASE-XDR8 OSFP PAM4 1310nm 2km DOM MTP/MPO-16 SMF Optical Transceiver
OSFP800-XDR8-B2	800GBASE-XDR8 OSFP PAM4 1310nm 2km DOM Dual MTP/MPO-12 SMF Optical Transceiver
OSFP800-2FR4-A2	800GBASE-2FR4 OSFP PAM4 1310nm 2km DOM LC SMF Optical Transceiver
OSFP800-2LR4-A2	800GBASE-2LR4 OSFP PAM4 1310nm 10km Dual LC SMF Optical Transceiver
OSFP800-PLR8-B2	800GBASE-PLR8 OSFP PAM4 1310nm 10km DOM Dual MTP/MPO-12 SMF Optical Transceiver
OSFP800-PLR8-B1	800GBASE-PLR8 OSFP PAM4 1310nm 10km DOM MTP/MPO-16 SMF Optical Transceiver
QDD800-PLR8-B1	800GBASE-PLR8 QSFP-DD PAM4 1310nm 10km DOM MTP/MPO-16 SMF Optical Transceiver



https://www.fs.com