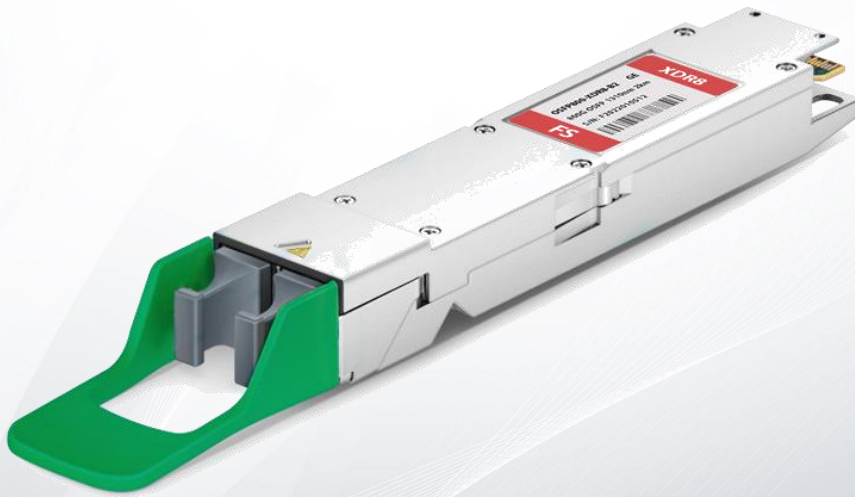


# 800GBASE-XDR8 OSFP 1310nm 2km Dual MTP/MPO-12 Transceiver

OSFP800-XDR8-B2



## Application

- 800G Ethernet
- Data Center
- Breakout 2x 400G XDR4
- Breakout 8x 100G FR

## Features

- Maximum Power Consumption 16.5W
- 8x106.25 Gb/s PAM4 Modulation
- Single 3.3V Power Supply
- Operating Case Temperature Range: 0 to +70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser Safety

## Standards

- Compliant with IEEE 802.3cu-2021  
-8x100GBASE-FR1 Optical Interface
- Compliant with IEEE P802.3ck D3.0  
-8x100GAUI-1 C2M Electrical Interface
- Compliant with OSFP MSA HW Rev 4.1  
-Type 2 Housing with Dual MPO-12 Connector
- Compliant with CMIS Rev 5.0

## Description

FS's 800GBASE-XDR8 OSFP transceiver supports up to 2km link lengths over single-mode fiber (SMF) via dual MTP/MPO-12 connectors. This transceiver is compliant with IEE802.3ck, IEEE 802.3cu-2021, OSFP MSA and CMIS Rev 5.0 standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 2x 400G XDR4 or 8x 100G FR, 800G Ethernet and Data Center applications.

## Products Specifications

### I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
<b>Storage Temperature</b>	$T_S$	-40	85	°C
<b>Supply Voltage</b>	$V_{CC}$	-0.5	3.6	V
<b>Relative Humidity (Non-condensing)</b>	RH	5	95	%
<b>Data Input Voltage Differential</b>	$ V_{DIP} - V_{DIN} $		1	V
<b>Control Input Voltage</b>	$V_I$	-0.3	$V_{CC} + 0.5$	V
<b>Control Output Current</b>	$I_O$	-20	20	mA

## II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Operating Case Temperature</b>	$T_{OPR}$	0		70	°C
<b>Power Supply Voltage</b>	$V_{CC}$	3.135	3.3	3.465	V
<b>Instantaneous Peak Current at Hot Plug</b>	$I_{CC\_IP}$			TBD	mA
<b>Sustained Peak Current at Hot Plug</b>	$I_{CC\_SP}$			TBD	mA
<b>Maximum Power Dissipation</b>	$P_D$			16.5	W
<b>Maximum Power Dissipation, Low Power Mode</b>	$P_{DLP}$			2	W
<b>Signalling Speed per Lane</b>	DRL		53.125		GBd
<b>Control Input Voltage High</b>	$V_{IH}$	$V_{CC} * 0.7$		$V_{CC} + 0.3$	V
<b>Control Input Voltage Low</b>	$V_{IL}$	-0.3		$V_{CC} * 0.3$	V
<b>Two Wire Serial Interface Clock Rate</b>				400	kHz
<b>Power Supply Noise 1 kHz -1 MHz (p-p)</b>				66	mVpp
<b>Operating Distance</b>		2		2000	m

### III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Transmitter</b>						
<b>Wavelength</b>	$\lambda_c$	1304.5	1311	1317.5	nm	
<b>Side Mode Suppression Ratio</b>	SMSR	30			dB	
<b>Average Launch Power, each Lane</b>	$AOP_L$	-3.1		4.0	dBm	1
<b>Outer Optical Modulation Amplitude (<math>OMA_{outer}</math>), each Lane for <math>TDECQ &lt; 1.4\text{dB}</math> for <math>1.4\text{dB} \leq TDECQ \leq 3.4\text{dB}</math></b>	$OMA_{outer}$	-0.1 $-1.5 + TDECQ$		4.2	dBm	
<b>Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane</b>	TDECQ			3.4	dB	
<b>Transmitter Eye Closure for PAM4 (TECQ), each Lane</b>	TECQ			3.4	dB	
<b> TDECQ-TECQ </b>				2.5	dB	
<b>Over/Under-shoot</b>				22	%	
<b>Transmitter Power Excursion</b>				2	dBm	
<b>Average Launch Power of OFF Transmitter, each Lane</b>	$T_{OFF}$			-15	dBm	
<b>Extinction Ratio</b>	ER	3.5			dB	
<b>Transmitter Transition Time</b>	$T_r$			17	ps	
<b><math>RIN_{15.6OMA}</math></b>	RIN			-136	dB/Hz	
<b>Optical Return Loss Tolerance</b>	ORL			17.1	dB	
<b>Transmitter Reflectance</b>	TR			-26	dB	2

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
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### Receiver

<b>Wavelength</b>	$\lambda_{CO}$	1304.5	1311	1317.5	nm	
<b>Damage Threshold, each Lane</b>	$AOP_D$	5			dBm	
<b>Average Receive Power, each Lane</b>	$AOP_R$	-7.1		4	dBm	
<b>Receive Power (OMAouter), each Lane</b>	$OMA_R$			4.2	dBm	
<b>Receiver Reflectance</b>	RR			-26	dB	
<b>Receiver Sensitivity (OMAouter) for <math>TECQ &lt; 1.4</math> dB for <math>1.4 \text{ dB} \leq TECQ \leq 3.4</math> dB</b>	$S_{OMA}$			-4.5 -5.9 + TECQ	dBm	3
<b>Stressed Receiver Sensitivity (OMAouter), each Lane</b>	SRS			-2.5	dBm	4

### Conditions of Stressed Receiver Sensitivity Test

<b>Stressed Eye Closure for PAM4 (SECQ), Lane Under Test</b>	SECQ		3.4		dB	
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**NOTE 1:** Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

**NOTE 2:** Transmitter reflectance is defined looking into the transmitter.

**NOTE 3:** Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

**NOTE 4:** Measured with conformance test signal at TP3 for the BER =  $2.4 \times 10^{-4}$ .

## IV. Electrical Characteristics

### 1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

Parameter	Symbol	Min.	Typical	Max.	Unit
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#### Receiver (Module Output, TP4)

AC Common-mode Output Voltage (RMS)				25	mV
Differential Peak-to-peak Output Voltage	Short Mode			600	mV
	Long Mode			845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLD <sub>c</sub>		802.3ck 120G-1		dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V

#### Transmitter (Module Input, TP1)

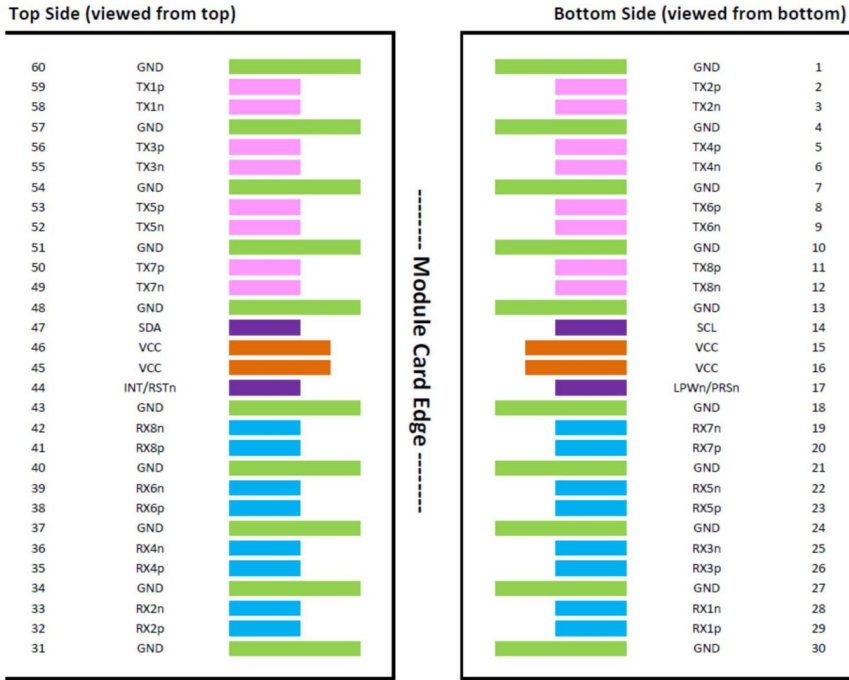
Differential Pk-pk Input Voltage Tolerance (TP1a)		750			mV
AC Common-mode RMS Voltage Tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RL <sub>cd</sub>		802.3ck 120G-2		dB
Effective Return Loss	ERL	8.5			dB

Parameter	Symbol	Min.	Typical	Max.	Unit
<b>Differential Termination Mismatch</b>				10	%
<b>Single-ended Voltage Tolerance Range</b>		-0.4		3.3	V
<b>DC Common-mode Voltage Tolerance</b>		-0.35		2.85	V

## 2. Electrical Specification Low Speed Control and Sense Signals(Compliant with QSFP-DD HW Rev6.01 Table 14)

Parameter	Symbol	Min.	Max.	Unit
<b>Module Output SCL and SDA</b>	$V_{OL}$	0	0.4	V
<b>Module Input SCL and SDA</b>	$V_{IL}$	-0.3	$V_{CC} * 0.3$	V
	$V_{IH}$	$V_{CC} * 0.7$	$V_{CC} + 0.5$	V
<b>InitMode, ResetL and ModSelL</b>	$V_{IL}$	-0.3	0.8	V
	$V_{IH}$	2	$V_{CC} + 0.3$	V
<b>IntL</b>	$V_{OL}$	0	0.4	V
	$V_{OH}$	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V

## V. Pin Description



Pin	Symbol	Description	Logic
1	GND	Ground	
2	TX2p	Transmitter Data Non-Inverted	CML-I
3	TX2n	Transmitter Data Inverted	CML-I
4	GND	Ground	
5	TX4p	Transmitter Data Non-Inverted	CML-I
6	TX4n	Transmitter Data Inverted	CML-I
7	GND	Ground	
8	TX6p	Transmitter Data Non-Inverted	CML-I
9	TX6n	Transmitter Data Inverted	CML-I

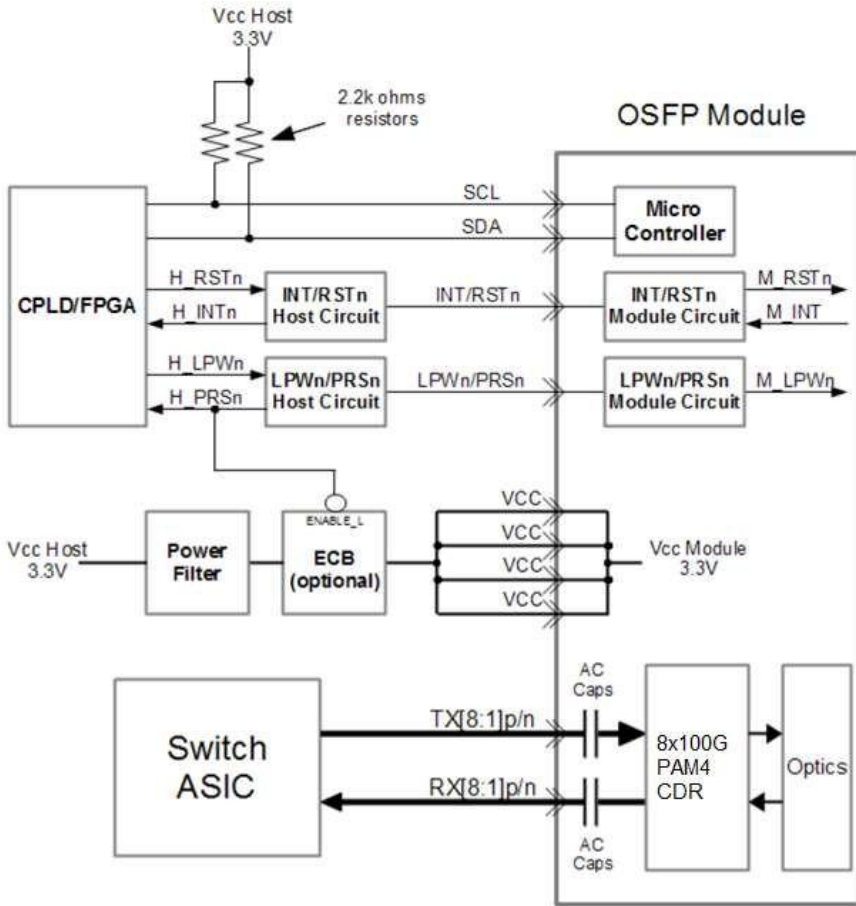


Pin	Symbol	Description	Logic
10	GND	Ground	
11	TX8p	Transmitter Data Non-Inverted	CML-I
12	TX8n	Transmitter Data Inverted	CML-I
13	GND	Ground	
14	SCL	2-wire Serial Interface Clock	LVC MOS-I/O
15	V <sub>CC</sub>	+3.3V Power	
16	V <sub>CC</sub>	+3.3V Power	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level
18	GND	Ground	
19	RX7n	Receiver Data Inverted	CML-O
20	RX7p	Transmitter Data Non-Inverted	CML-O
21	GND	Ground	
22	RX5n	Receiver Data Inverted	CML-O
23	RX5p	Receiver Data Non-Inverted	CML-O
24	GND	Ground	
25	RX3n	Receiver Data Inverted	CML-O
26	RX3p	Receiver Data Non-Inverted	CML-O
27	GND	Ground	

Pin	Symbol	Description	Logic
28	RX1n	Receiver Data Inverted	CML-O
29	RX1p	Receiver Data Non-Inverted	CML-O
30	GND	Ground	
31	GND	Ground	
32	RX2p	Receiver Data Non-Inverted	CML-O
33	RX2n	Receiver Data Inverted	CML-O
34	GND	Ground	
35	RX4p	Receiver Data Non-Inverted	CML-O
36	RX4n	Receiver Data Inverted	CML-O
37	GND	Ground	
38	RX6p	Receiver Data Non-Inverted	CML-O
39	RX6n	Receiver Data Inverted	CML-O
40	GND	Ground	
41	RX8p	Receiver Data Non-Inverted	CML-O
42	RX8n	Receiver Data Inverted	CML-O
43	GND	Ground	
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level
45	V <sub>CC</sub>	3.3V Power	

Pin	Symbol	Description	Logic
46	V <sub>CC</sub>	3.3V Power	
47	SDA	2-wire Serial Interface Data	LVCMOS-I/O
48	GND	Ground	
49	TX7n	Transmitter Data Inverted	CML-I
50	TX7p	Transmitter Data Non-Inverted	CML-I
51	GND	Ground	
52	TX5n	Transmitter Data Inverted	CML-I
53	TX5p	Transmitter Data Non-Inverted	CML-I
54	GND	Ground	
55	TX3n	Transmitter Data Inverted	CML-I
56	TX3p	Transmitter Data Non-Inverted	CML-I
57	GND	Ground	
58	TX1n	Transmitter Data Inverted	CML-I
59	TX1p	Transmitter Data Non-Inverted	CML-I
60	GND	Ground	

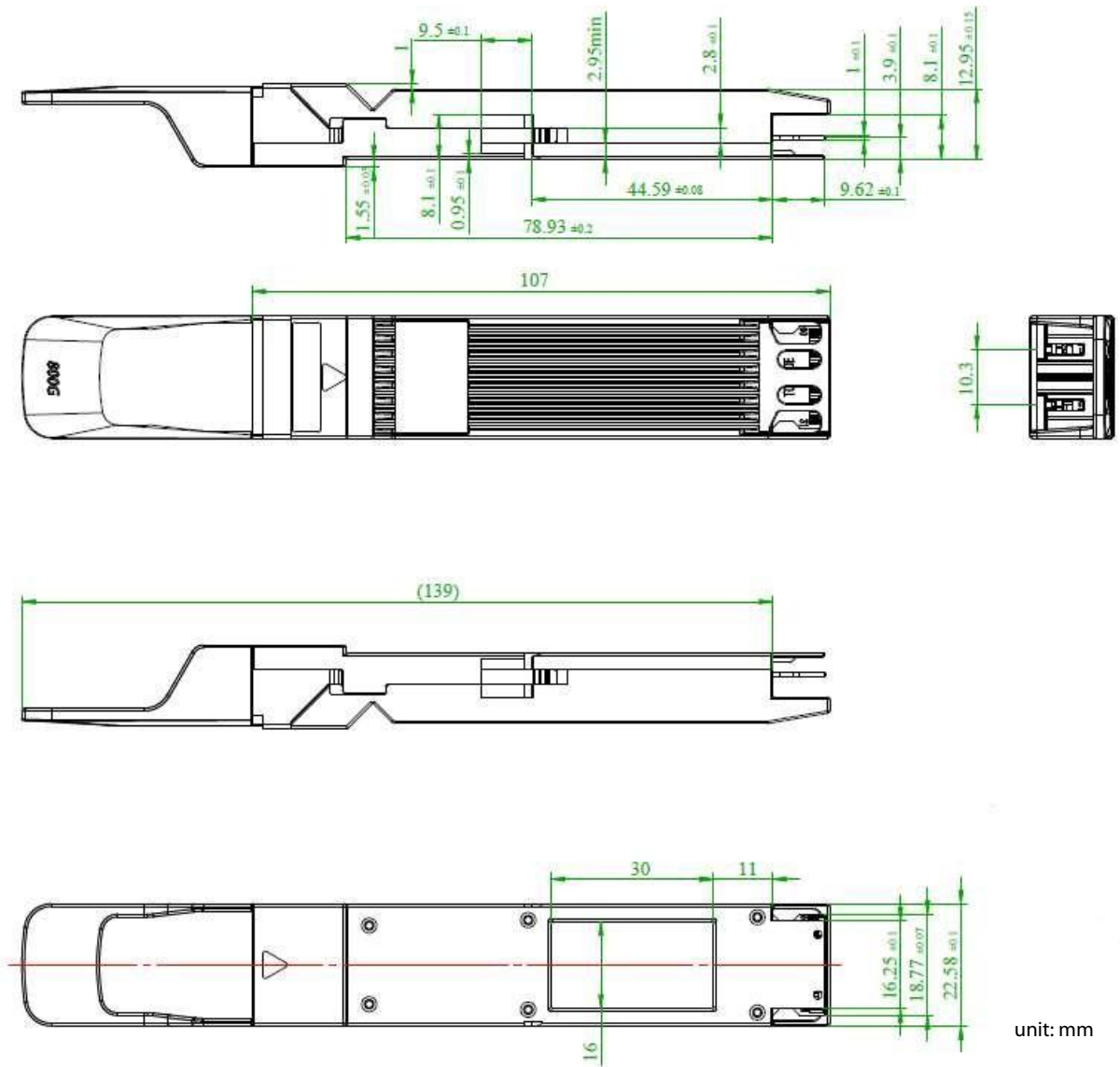
## VI. Recommended OSFP Host Board Schematic



## VII. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
<b>Temperature</b>	0 to 70	±3	°C	Internal
<b>Voltage</b>	0 to $V_{CC}$	0.1	V	Internal
<b>Tx Bias Current (each Lane)</b>	0 to 100	10%	mA	Internal
<b>Tx Output Power (each Lane)</b>	-3.1 to +4	±3	dB	Internal
<b>Rx Receive Power (each Lane)</b>	-7.1 to +4	±3	dB	Internal

### VIII. Diagram Mechanical Drawing



## Order Information

Part Number	Description
QDD800-DR8-B1	800GBASE-DR8 QSFP-DD PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver
QDD800-2FR4-C1	800GBASE-2FR4 QSFP-DD PAM4 1310nm 2km DOM Dual CS SMF Optical Transceiver
OSFP800-DR8-B1	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver
OSFP800-DR8-B2	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO SMF Optical Transceiver
OSFP800-XDR8-B1	800GBASE-XDR8 OSFP PAM4 1310nm 2km DOM MTP/MPO-16 SMF Optical Transceiver
OSFP800-XDR8-B2	800GBASE-XDR8 OSFP PAM4 1310nm 2km DOM Dual MTP/MPO-12 SMF Optical Transceiver
OSFP800-2FR4-A2	800GBASE-2FR4 OSFP PAM4 1310nm 2km DOM LC SMF Optical Transceiver
OSFP800-PLR8-B2	800GBASE-PLR8 OSFP PAM4 1310nm 10km DOM Dual MTP/MPO-12 SMF Optical Transceiver



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