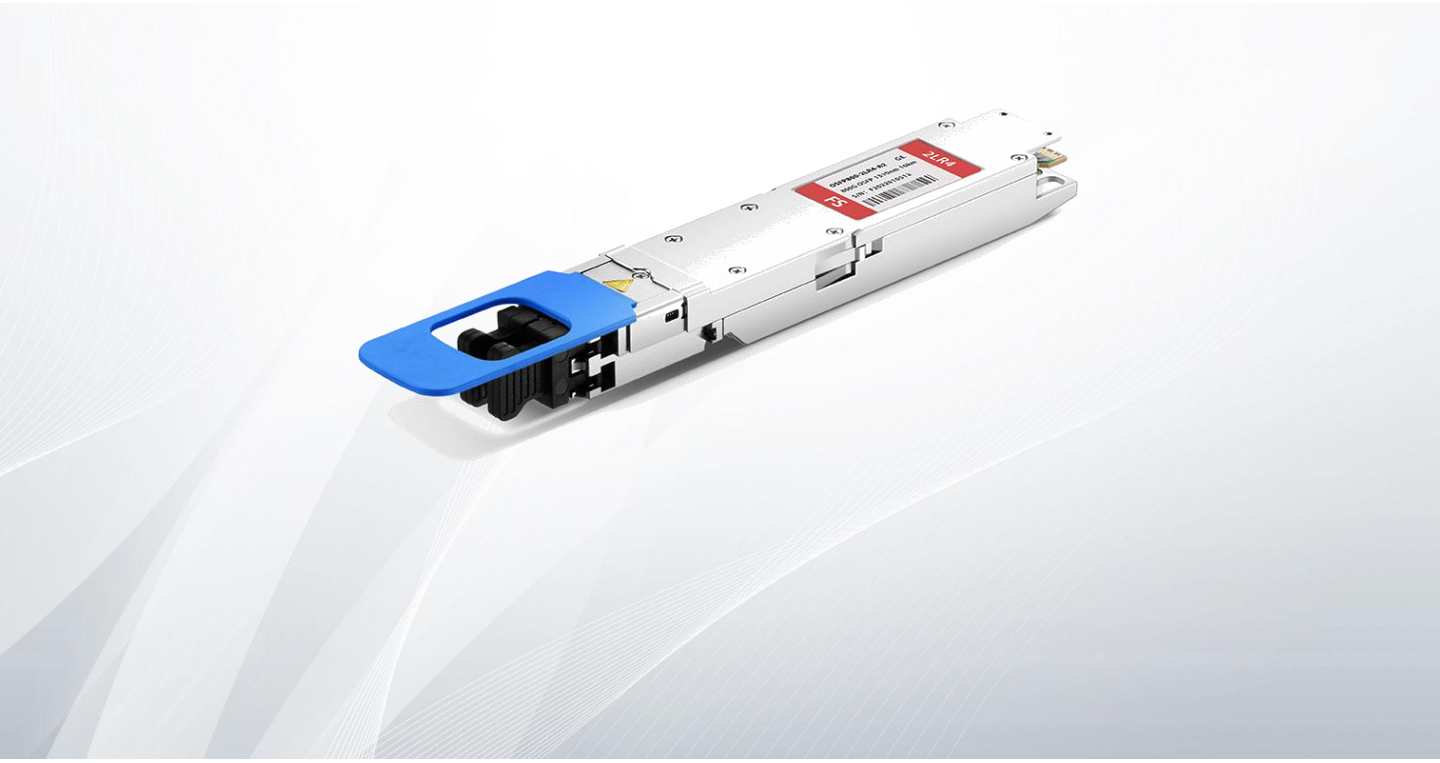
800GBASE-2LR4 OSFP 1310nm 10km Dual LC Duplex Transceiver

OSFP800-2LR4-A2



Application

- 800G Ethernet
- Data Center
- Breakout 2x 400G LR4

Features

- Maximum Power Consumption 18W
- 8x106.25 Gb/s PAM4 Modulation
- Single 3.3V Power Supply
- Operating Case Temperature Range: 0 to +70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Class 1 Laser Safety

Standards

- Compliant with MSA
  -2x400G-LR4-10 Optical Interface
- Compliant with IEEE P802.3ck D3.0
  -2x400GAUI-4 C2M Electrical Interface
- Compliant with OSFP MSA HW Rev 4.1
  -Type 2 Housing with Dual LC Connector
- Compliant with CMIS Rev 5.0

Description

FS's 800GBASE-2LR4 OSFP transceiver supports up to 10km link lengths over single-mode fiber (SMF) via dual LC connectors. This transceiver is compliant with IEEE 802.3ck, OSFP MSA and CMIS Rev 5.0 standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet, Breakout 2x 400G LR4 and Data Center applications.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
Data Input Voltage Differential	$\|V_{DIP}-V_{DIN}\|$		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_{OPR}	0		70	ºC
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			TBD	mA
Sustained Peak Current at Hot Plug	I_{CC_SP}			TBD	mA

Parameter	Symbol	Min.	Typical	Max.	Unit
Maximum Power Dissipation	P_D		16	18	W
Maximum Power Dissipation, Low Power Mode	P_{DLP}			2	W
Signalling Speed per Lane	DRL		53.125		GBd
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V
Two Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise 1 kHz -1 MHz (p-p)				66	mVpp
Operating Distance		2		10000	m

III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength L0, L4	λ_{C0}, λ_{C4}	1264.5	1271	1277.5	nm	
Wavelength L1, L5	λ_{C1}, λ_{C5}	1284.5	1291	1297.5	nm	
Wavelength L2, L6	λ_{C2}, λ_{C6}	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λ_{C3}, λ_{C7}	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power (Max.)	AOP_T			11.1	dBm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Average Launch Power, each Lane	AOP_L	-2.7		5.1	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane for TDECQ<1.4dB for1.4dB<= TDECQ<=3.4dB	T_{OMA}	0.3 –1.1 + TDECQ		4.4	dBm	
Difference in Launch Power Between Any Two Lanes (OMA_{outer})	AOP_d			4	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.9	dB	
Transmitter Eye Closure for PAM4 (TECQ), each Lane	TECQ			3.9	dB	
|TDECQ-TECQ|				2.5	dB	
Transmitter Over/Under-shoot				25	%	
Transmitter Power Excursion				5.2	dBm	
Average Launch Power of OFF Transmitter, each Lane	T_{OFF}			-16	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time(Max.)	Tr			17	ps	
$RIN_{15.6}OMA$(Max.)	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.6	dB	
Transmitter Reflectance	TR			-26	dB	2
		Receiver				
Wavelength L0, L4	λ_{C0}, λ_{C4}	1264.5	1271	1277.5	nm	
Wavelength L1, L5	λ_{C1}, λ_{C5}	1284.5	1291	1297.5	nm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L2, L6	λ_{C2}, λ_{C6}	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λ_{C3}, λ_{C7}	1324.5	1331	1337.5	nm	
Damage Threshold, each Lane	AOP_D	6.1			dBm	
Average Receive Power, each Lane	AOP_R	-9		5.1	dBm	
Receive Power (OMA_{outer}), each Lane	OMA_R			4.4	dBm	
Difference in Receive Power Between Any Two Lanes (OMA_{outer})	AOP_g			4.3	dB	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA_{outer}) for TECQ<1.4 dB for 1.4dB<=TECQ<=3.4dB	S_{OMA}			-6.8 -8.2+TECQ	dBm	
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.3	dBm	3
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test			3.9		dB	
OMA_{outer} of Each Aggressor Lane			-0.4		dBm	

NOTE 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

NOTE 2: Transmitter reflectance is defined looking into the transmitter.

NOTE 3: Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$.

IV. Electrical Characteristics

1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

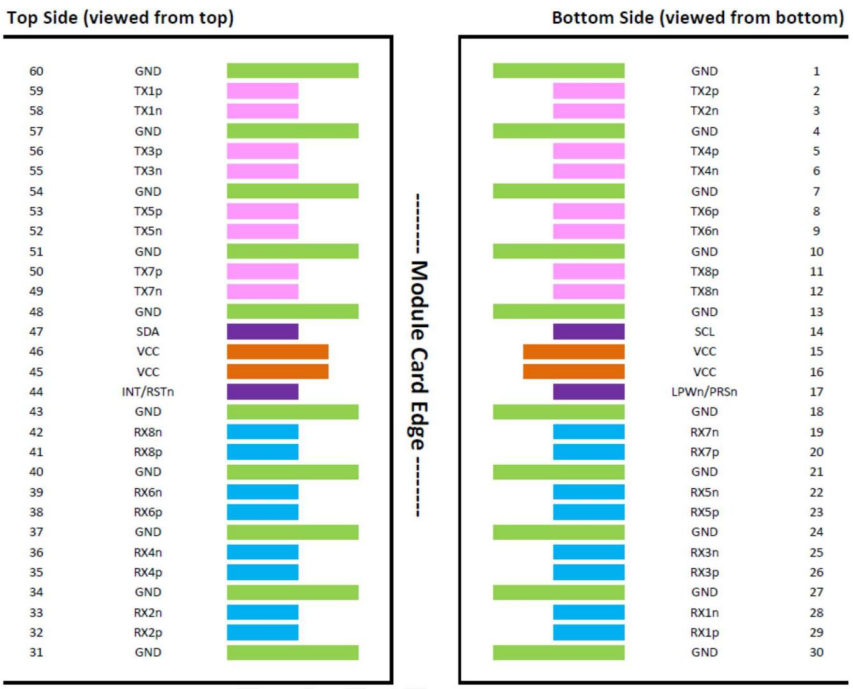
Parameter	Symbol	Min.	Typical	Max.	Unit
Receiver (Module Output, TP4)					
AC Common-mode Output Voltage (RMS)				25	mV
Differential Peak-to-peak Output Voltage — **Short Mode**				600	mV
Differential Peak-to-peak Output Voltage — **Long Mode**				845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLD_C		802.3ck 120G-1		dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Transmitter (Module Input, TP1)					
Differential Pk-pk Input Voltage Tolerance (TP1a)		750			mV
AC Common-mode RMS Voltage Tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RL_{cd}		802.3ck 120G-2		dB
Effective Return Loss	ERL	8.5			dB

Parameter	Symbol	Min.	Typical	Max.	Unit
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerance Range		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V

2. Electrical Specification Low Speed Control and Sense Signals (Compliant with QSFP-DD HW Rev6.01 Table 14)

Parameter	Symbol	Min.	Max.	Unit
Module Output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	V_{CC}+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V

V. Pin Description



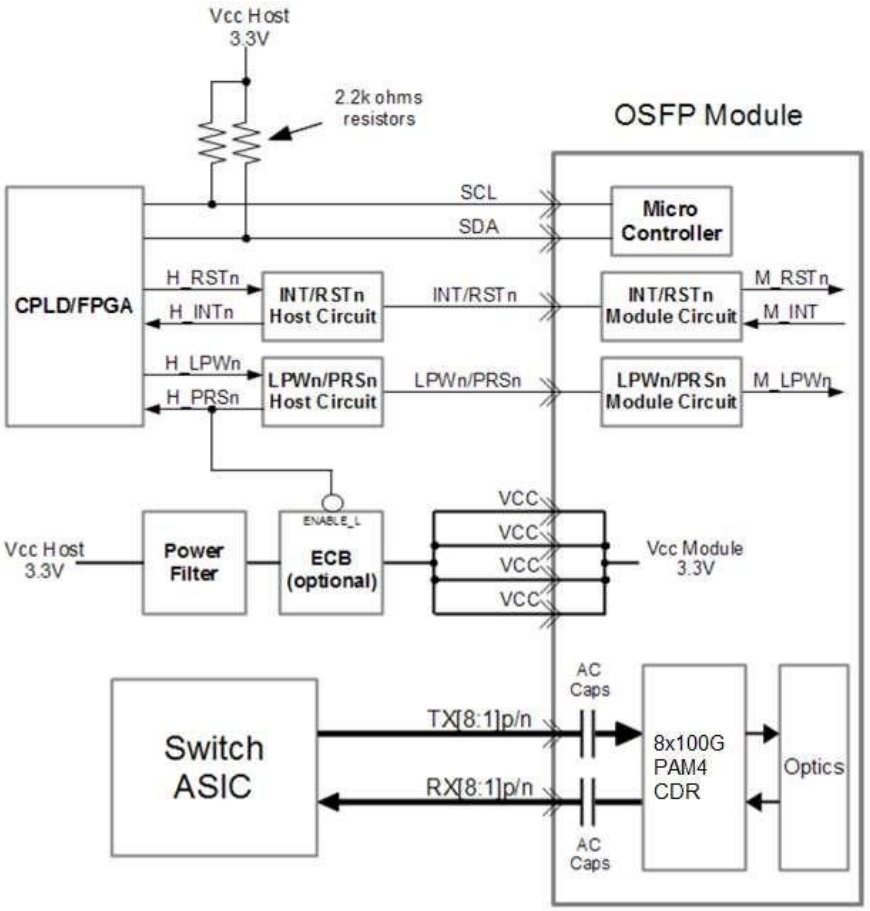
Pin	Symbol	Description	Logic
1	GND	Ground	
2	TX2p	Transmitter Data Non-Inverted	CML-I
3	TX2n	Transmitter Data Inverted	CML-I
4	GND	Ground	
5	TX4p	Transmitter Data Non-Inverted	CML-I
6	TX4n	Transmitter Data Inverted	CML-I
7	GND	Ground	
8	TX6p	Transmitter Data Non-Inverted	CML-I
9	TX6n	Transmitter Data Inverted	CML-I

Pin	Symbol	Description	Logic
10	GND	Ground	
11	TX8p	Transmitter Data Non-Inverted	CML-I
12	TX8n	Transmitter Data Inverted	CML-I
13	GND	Ground	
14	SCL	2-wire Serial Interface Clock	LVCMOS-I/O
15	V_{CC}	+3.3V Power	
16	V_{CC}	+3.3V Power	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level
18	GND	Ground	
19	RX7n	Receiver Data Inverted	CML-O
20	RX7p	Transmitter Data Non-Inverted	CML-O
21	GND	Ground	
22	RX5n	Receiver Data Inverted	CML-O
23	RX5p	Receiver Data Non-Inverted	CML-O
24	GND	Ground	
25	RX3n	Receiver Data Inverted	CML-O
26	RX3p	Receiver Data Non-Inverted	CML-O
27	GND	Ground	

Pin	Symbol	Description	Logic
28	RX1n	Receiver Data Inverted	CML-O
29	RX1p	Receiver Data Non-Inverted	CML-O
30	GND	Ground	
31	GND	Ground	
32	RX2p	Receiver Data Non-Inverted	CML-O
33	RX2n	Receiver Data Inverted	CML-O
34	GND	Ground	
35	RX4p	Receiver Data Non-Inverted	CML-O
36	RX4n	Receiver Data Inverted	CML-O
37	GND	Ground	
38	RX6p	Receiver Data Non-Inverted	CML-O
39	RX6n	Receiver Data Inverted	CML-O
40	GND	Ground	
41	RX8p	Receiver Data Non-Inverted	CML-O
42	RX8n	Receiver Data Inverted	CML-O
43	GND	Ground	
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level
45	V_{CC}	3.3V Power	

Pin	Symbol	Description	Logic
46	V_{CC}	3.3V Power	
47	SDA	2-wire Serial Interface Data	LVCMOS-I/O
48	GND	Ground	
49	TX7n	Transmitter Data Inverted	CML-I
50	TX7p	Transmitter Data Non-Inverted	CML-I
51	GND	Ground	
52	TX5n	Transmitter Data Inverted	CML-I
53	TX5p	Transmitter Data Non-Inverted	CML-I
54	GND	Ground	
55	TX3n	Transmitter Data Inverted	CML-I
56	TX3p	Transmitter Data Non-Inverted	CML-I
57	GND	Ground	
58	TX1n	Transmitter Data Inverted	CML-I
59	TX1p	Transmitter Data Non-Inverted	CML-I
60	GND	Ground	

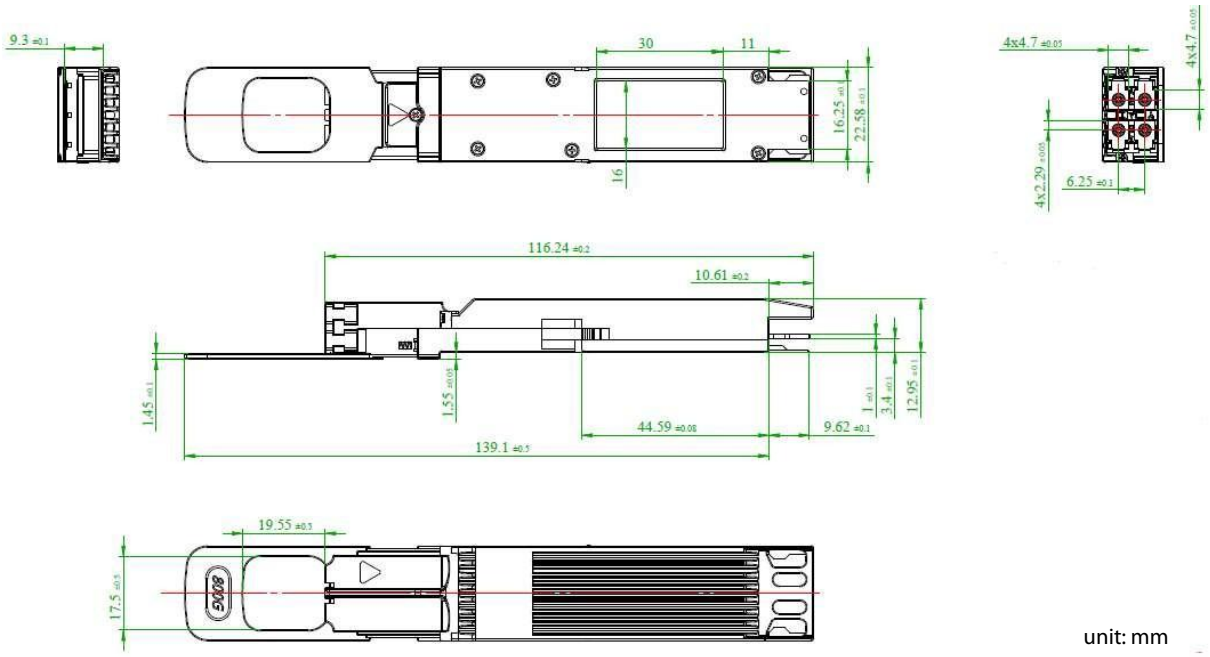
VI. Recommended OSFP Host Board Schematic



VII. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (each Lane)	-2.7 to +5.1	±3	dB	Internal
Rx Receive Power (each Lane)	-9 to +5.1	±3	dB	Internal

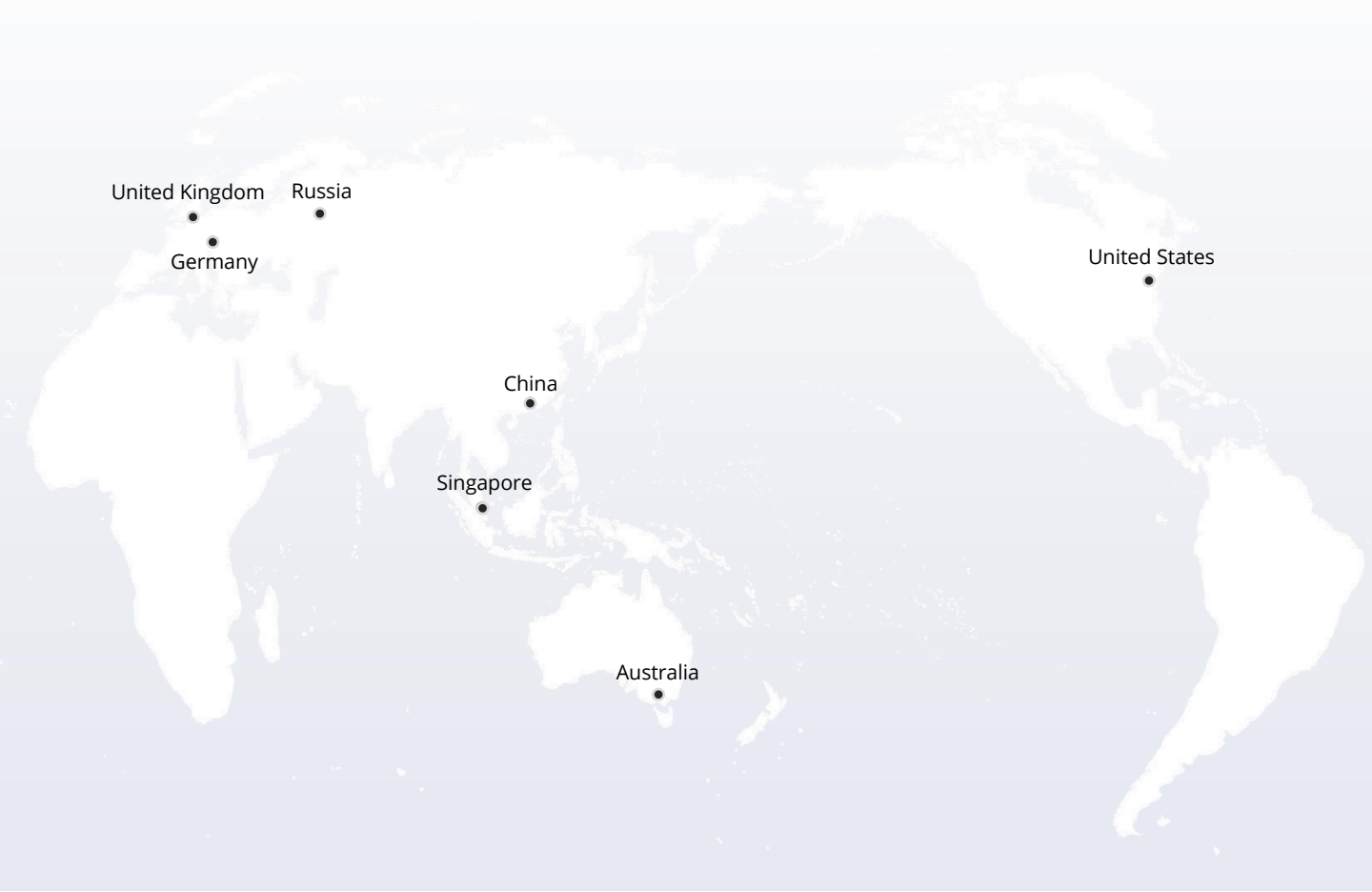
VIII. Diagram Mechanial Drawing



unit: mm

Order Information

Part Number	Description
QDD800-DR8-B1	800GBASE-DR8 QSFP-DD PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver
QDD800-2FR4-C1	800GBASE-2FR4 QSFP-DD PAM4 1310nm 2km DOM Dual CS SMF Optical Transceiver
OSFP800-DR8-B1	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver
OSFP800-DR8-B2	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO SMF Optical Transceiver
OSFP800-XDR8-B1	800GBASE-XDR8 OSFP PAM4 1310nm 2km DOM MTP/MPO-16 SMF Optical Transceiver
OSFP800-XDR8-B2	800GBASE-XDR8 OSFP PAM4 1310nm 2km DOM Dual MTP/MPO-12 SMF Optical Transceiver
OSFP800-2FR4-A2	800GBASE-2FR4 OSFP PAM4 1310nm 2km DOM LC SMF Optical Transceiver
OSFP800-2LR4-A2	800GBASE-2LR4 OSFP PAM4 1310nm 10km Dual LC SMF Optical Transceiver
OSFP800-PLR8-B2	800GBASE-PLR8 OSFP PAM4 1310nm 10km DOM Dual MTP/MPO-12 SMF Optical Transceiver



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