800GBASE-DR8 QSFP-DD 1310nm 500m MTP/MPO-16 SMF Transceiver

QDD800-DR8-B1

Application

- 800G Ethernet
- Data Center

Standards

- Compliant with IEEE 802.3cu-2021
  -8x100GBASE-DR Optical Interface
- Compliant with IEEE P802.3ck D3.0
  -8x100GAUI-1 C2M Electrical Interface
- Compliant with QSFP-DD MSA HW Rev 6.01
  -Type 2A with MPO-16 Connector
- Compliant with CMIS Rev 5.0

Features

- Maximum Power Consumption :16.5W
- Case Operating Temperature 0℃ to 70℃
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU
- Class 1 Laser Safety

Description

The 800GBASE-DR8 QSFP-DD transceiver is designed for 800GBASE Ethernet throughput up to 500m over singlemode fiber (SMF) with MPO-16 connectors. This transceiver is compliant with IEEE P802.3ck, IEEE 802.3cu, QSFP-DD MSA. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.
It is suitable for 800G Ethernet, Data Center, Breakout 2x 400G DR4 or 8x 100G DR application.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (Non-condensing)	RH	5	95	%
Data Input Voltage Differential	IV_{DIP}-$V_{DIN}I$		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

II. Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	ºC	1
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	I_{CC_IP}			TBD	mA	
Sustained Peak Current at Hot Plug	I_{CC_SP}			TBD	mA	
Maximum Power Dissipation	P_D			16.5	W	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Maximum Power Dissipation, Low Power Mode	P_{DLP}			TBD	W	
Signalling Speed per Lane	DRL		53.125		GBd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz -1 MHz (p-p)				66	mVpp	
Operating Distance		2		500	m	

III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	AOP_L	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	T_{OMA}	-0.8		4.2	dBm	
Launch power in OMAouter Minus TDECQ, each Lane for Extinction Ratio >= 5 dB for Extinction Ratio < 5 dB	$T_{OMA-TDECQ}$	-2.2 -1.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
TDECQ – 10log10(Ceq), each Lane	Ceq			3.4	dB	
Average Launch Power of OFF Transmitter, each Lane	T_{OFF}			-15	dBm	

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time	Tr			17	ps	
$RIN_{15.5}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.5	dB	
Transmitter Reflectance	T_R			-26	dB	2
Receiver						
Wavelength	λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOP_D	5			dBm	
Average Receive Power, each Lane	AOP_R	-5.9		4	dBm	
Receive Power (OMAouter), each Lane	OMA_R			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMAouter), each Lane	S_{OMA}			Max(-3.9, SECQ -5.3)	dBm	3
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-1.9	dBm	4
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test	SECQ		3.4		dB	
SECQ – 10log10(Ceq), Lane Under Test	Ceq			3.4	dB	
OMAouter of each Aggressor Lane			4.2		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.

3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

4. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$.

IV. Electrical Characteristics

1. Electrical Specification High Speed Signal (Compliant with IEEE802.3ck C2M)

Parameter	Symbol	Min.	Typical	Max.	Unit
Receiver (Module Output, TP4)					
AC Common-mode Output Voltage (RMS)				25	mV
Differential peak-to-peak Output Voltage **Short Mode** **Long Mode**				600 845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLDc		802.3ck 120G-1		dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Transmitter (Module Input, TP1)					
Differential pk-pk Input Voltage Tolerance (TP1a)		750			mV
AC Common-mode RMS Voltage Tolerance (TP1a)		25			mV
Differential-mode to Common-mode Return Loss	RLcd		802.3ck 120G-2		dB

Parameter	Symbol	Min.	Typical	Max.	Unit
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerance Range		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V

2. Electrical Specification Low Speed Control and Sense Signals (Compliant with QSFP-DD HW Rev 6.01)

Parameter	Symbol	Min.	Max.	Unit
Module Output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	V_{CC}+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V

V. Pin Description

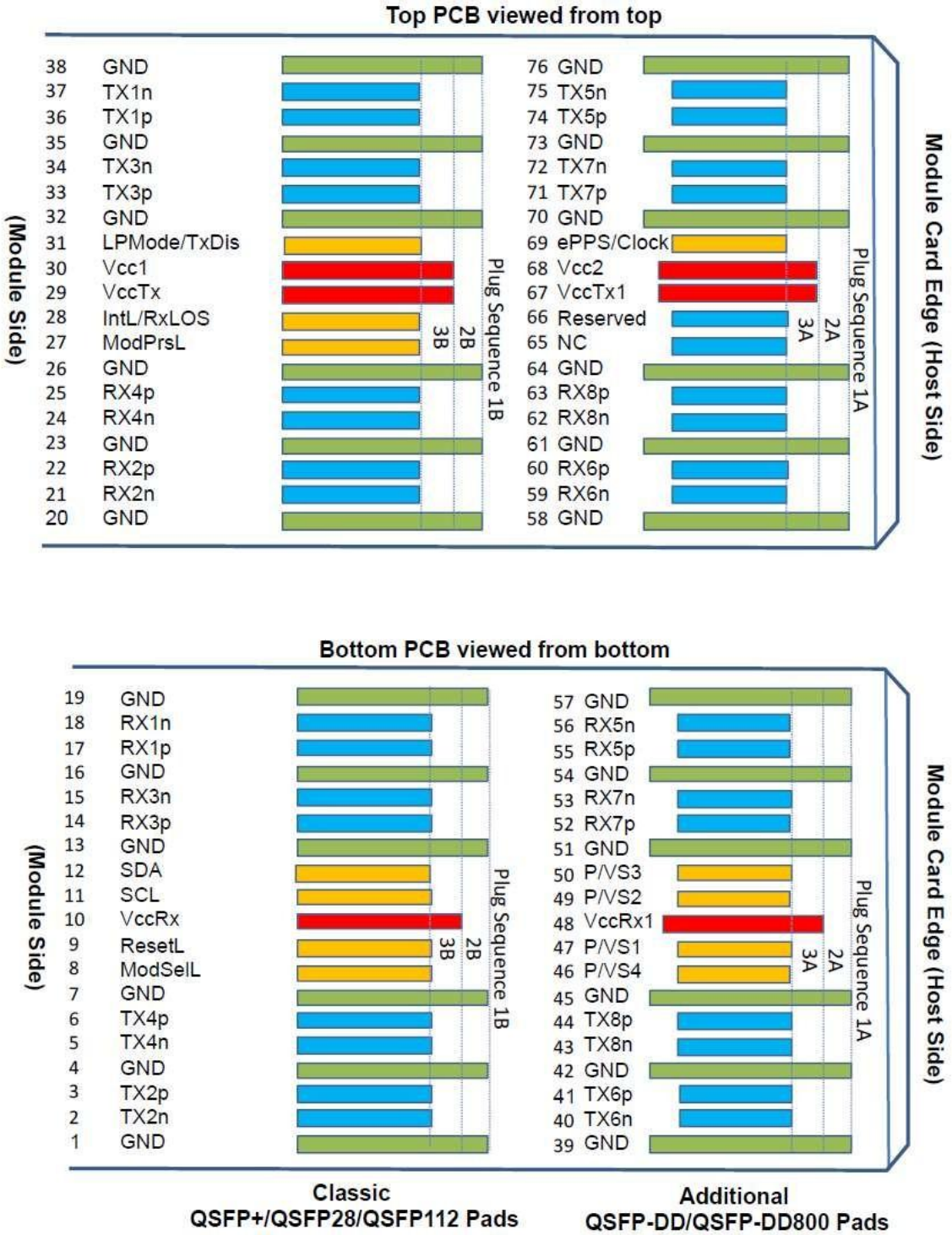


Figure 1 – Pin definitions of the module high speed inputs/outputs

Pin#	Logic	Symbol	Description	Pin#	Logic	Symbol	Description
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/CML-I	P/VS4	Programmable/ Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS/CML-I	P/VS1	Programmable/ Module Vendor Specific1
10		VccRx	3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	TWI Serial Interface Clock	49	LVCMOS/CML-O	P/VS2	Programmable/ Module Vendor Specific2
12	LVCMOS-I/O	SDA	TWI Serial Interface Data	50	LVCMOS/CML-O	P/VS3	Programmable/ Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output

Pin#	Logic	Symbol	Description	Pin#	Logic	Symbol	Description
19		GND	Ground	**57**		GND	Ground
20		GND	Ground	**58**		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	**59**	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	**60**	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	**61**		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	**62**	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	**63**	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	**64**		GND	Ground
27	LVTTL-O	$ModP_{rs}L$	Module Present	**65**		NC	Not Connected
28	LVTTL-O	IntL/RxLOS	Interrupt/Optional Rx LOS	**66**		Reserved	
29		Vcc Tx	3.3V Power Supply Transmitter	**67**		VccTx1	3.3V Power Supply
30		Vcc 1	3.3V Power Supply	**68**		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/TxDis	Low Power Mode/Optional TX Disable	**69**	LVCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input
32		GND	Ground	**70**		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	**71**	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	**72**	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	**73**		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	**74**	CML-I	Tx5p	Transmitter Non-inverted Data Input

Pin#	Logic	Symbol	Description	Pin#	Logic	Symbol	Description
37	CML-I	Tx1n	Transmitter Inverted Data Input	**75**	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	**76**		GND	Ground

VI. Digital Diagnostic Functions

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0~70	±3	ºC	Internal
Voltage	0~V_{CC}	0.1	V	Internal
Tx Bias Current (each Lane)	0~100	10%	mA	Internal
Tx Output Power (each Lane)	-2.9~4	±3	dB	Internal
Rx Receive Power (each Lane)	-5.9~4	±3	dB	Internal

VII. Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

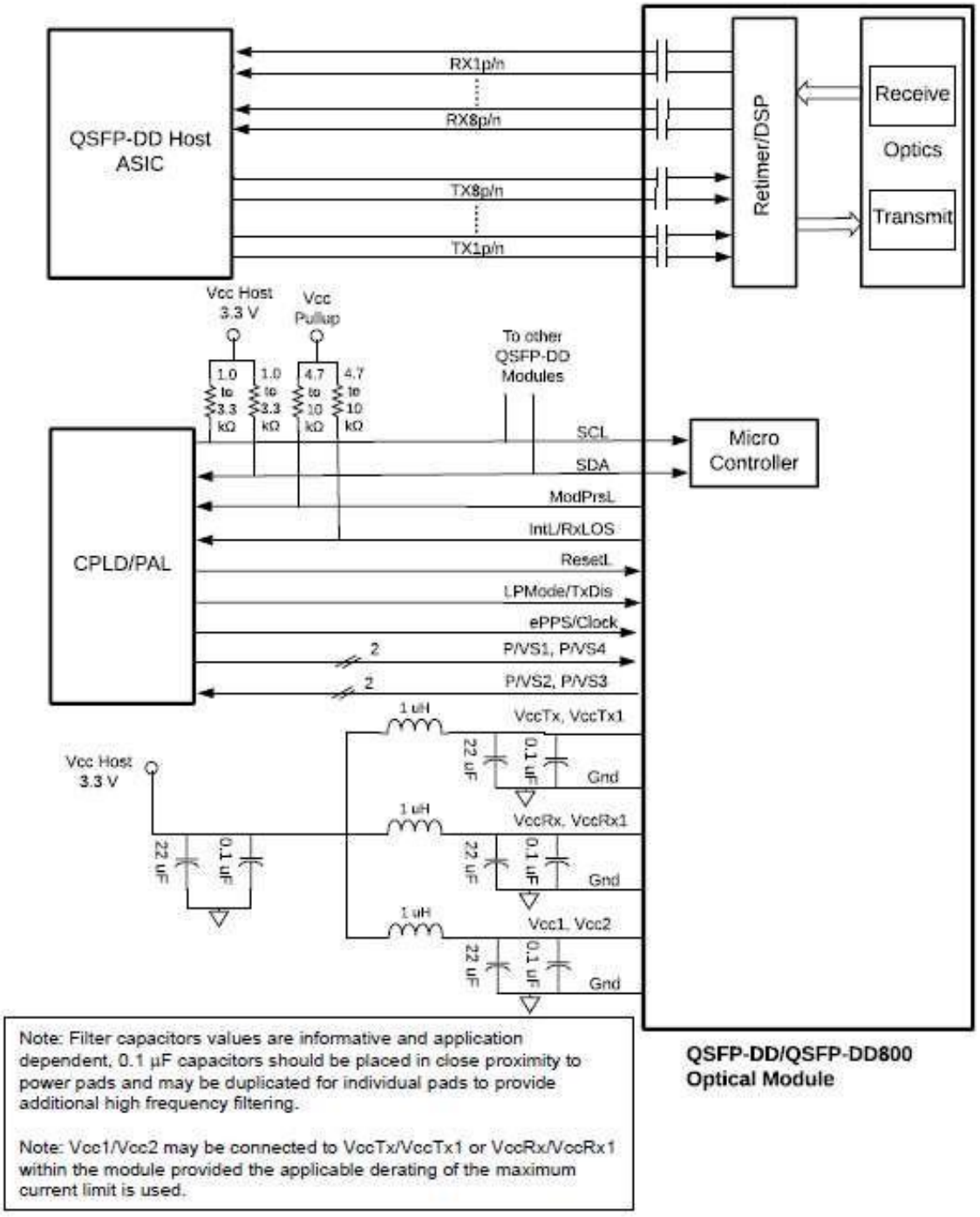
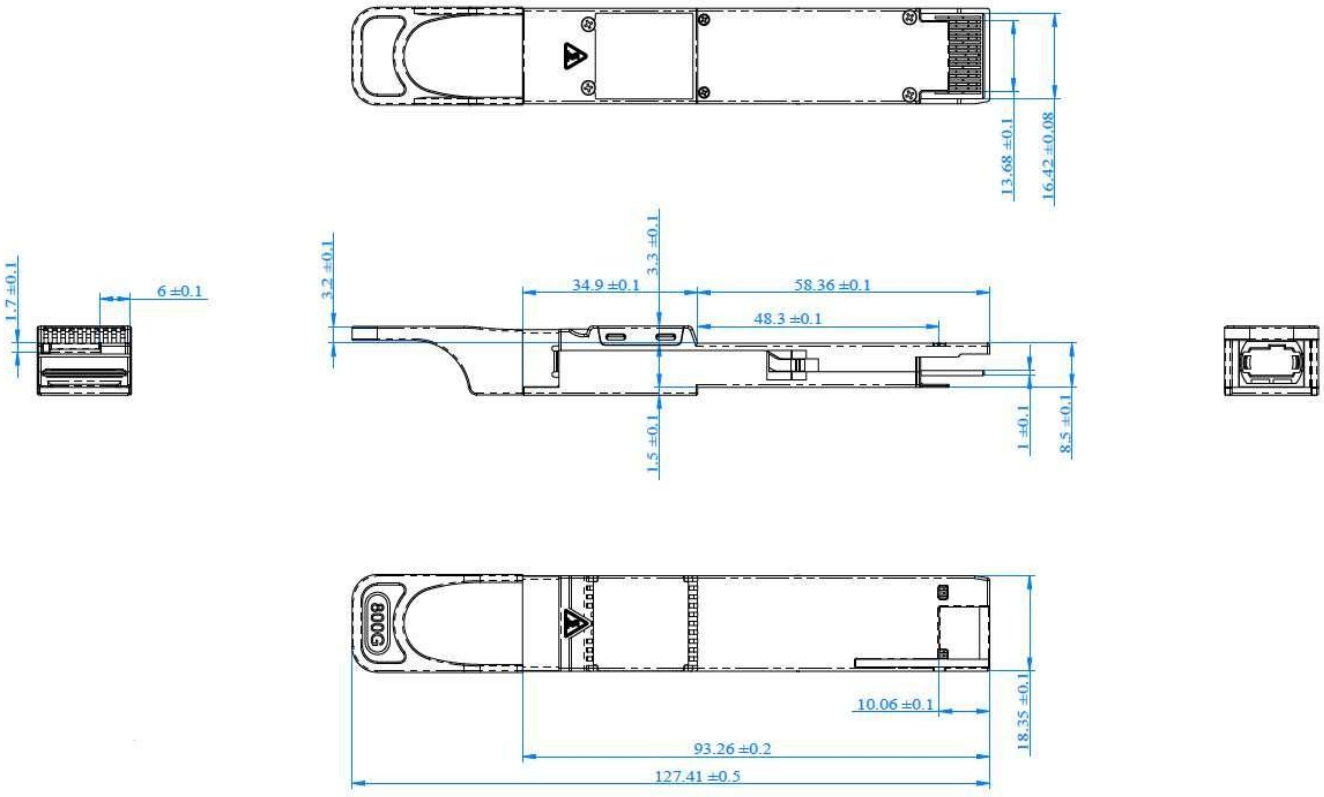


Figure 2 – Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

VIII. Mechanical Diagram



Order Information

Part Number	Description
OSFP800-DR8-B2	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO SMF Optical Transceiver
OSFP800-2FR4-A2	800GBASE-2FR4 OSFP PAM4 1310nm 2km DOM LC SMF Optical Transceiver
QDD800-2FR4-C1	800GBASE-2FR4 QSFP-DD PAM4 1310nm 2km DOM Dual CS SMF Optical Transceiver
OSFP800-XDR8-B1	800GBASE-XDR8 OSFP PAM4 1310nm 2km DOM MTP/MPO-16 SMF Optical Transceiver
OSFP800-PLR8-B2	800GBASE-PLR8 OSFP PAM4 1310nm 10km DOM Dual MTP/MPO-12 SMF Optical Transceiver
OSFP800-DR8-B1	800GBASE-DR8 OSFP PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver
QDD800-DR8-B1	800GBASE-DR8 QSFP-DD PAM4 1310nm 500m DOM MTP/MPO-16 SMF Optical Transceiver

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