FS

40G QSFP+ to QSFP+ Active Optical Cable (AOC)

Application

- 10G/40G Ethernet (10G/40GbE)
- 4G/ 8G/ 10G Fibre Channel
- PCI-Express, SAS/SATA, Fibre Channel compatible interconnect
- Proprietary high speed, high density data transmission
- Switch and router high speed backplane interconnect
- High performance computing, server and data storage

Features

- Full Duplex 4 Channel 850nm Parallel Active Optical Cable
- Transmission data rate up to 10.3Gbit/s per channel
- Reliable VCSEL and PIN photonic devices
- Hot pluggable electrical interface
- Differential AC-coupled high speed data interface
- Available lengths (in meters): 10, 20, 30, 40, 50...
- Commercial temperature range(COM): 0 to 70°C
- Single 3.3V power supply
- Low power consumption: less than 1.5 W per end
- I2C standard management interface
- Excellent high speed signal integrity
- Complies with QSFP+ MSA high-density form factor
- Compliant to industrial standard SFF-8436 QSFP+ active optical modules
- RoHS-6 Compliant

Description

FS.COM QSFP+ Active Optic Cables are a high performance, low power consumption, long reach interconnect solution supporting 40G Ethernet, fiber channel and PCIe. It is compliant with the QSFP+ MSA and IEEE P802.3ba 40GBASE-SR4.

FS.COM QSFP+ AOC is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10Gb/s, providing an aggregated rate of 40Gb/s. These AOCs can be used as an alternative solution to QSFP+ passive and active copper cables, while providing improved signal integrity, longer distances, superior electromagnetic immunity and better bit error rate performance.

Products Specifications

I. Absolute Maximum Ratings (V CC3=3.135V~3.465V, TC= 0°C to 70 °C, Per End)

*Exceeding the limits below may damage the active optical cable permanently.

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Operating Case Temperature	T_C	0		70	°C	
Ambient Humidity	H_A	5		85	%	1
Storage Ambient Humidity	H_A	0		85	%	
+3.3V Supply Voltage	V_{CC3}	3.135	3.3	3.465	V	
+3.3V Supply Current	I_{VCC3}			400	mA	
Total Power Dissipation	P_D			1.5	W	
Fiber Bend Radius	Rb	3			cm	
Bit rate	B	1		10.5	Gb/s	2
Module Turn-on Time				2000	ms	3
Input Control Voltage- High	ViH	2		Vcc+0.3	V	4
Input Control Voltage - Low	ViL	-0.3		0.8	V	4
Digital Output Voltage- High	VoH	2		Vcc+0.3		5
Digital Output Voltage- Low	VoL	0		0.8		5
Clock Rate-I2C				400	kHz	6

Notes:

1. Non-condensing

2. Tested with PRBS 231-1, BER 1X10^{-12}

3. Time from module power-on / insertion/ ResetL deassert to module full functional.

4. For all control input pins: LPMode, Reset and ModSelL

5. For all status output pins: ModPrsL, IntL

6. For management interface.

II. QSFP+ AOC Specifications

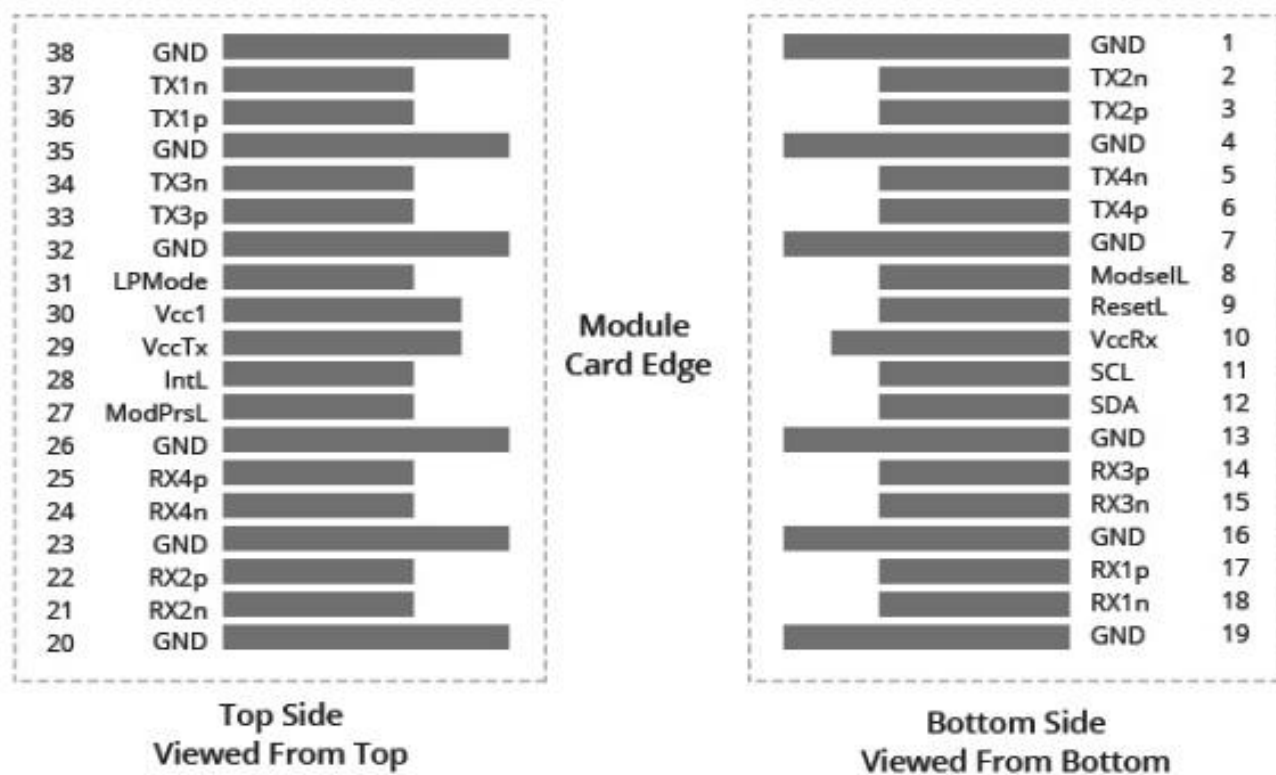| Parameter	Value	Unit	Notes
Module Form Factor	QSFP+		Supports SFF8431/SFF8432/SFF8472
Number of Lanes	4 Tx and 4 Rx		
Maximum Aggregate Data Rate	41.2	Gb/s	
Maximum Data Rate per Lane	10.3	Gb/s	No retimer or CDR devices embedded in the module. Allows operation at data-rates below 10.3 Gbps
Protocols Supported	Typical applications include Fibre Channel, 40G Ethernet, SATA/SAS3		
Bit Error Rate Performance	<10E-15		
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by the QSFP+ MSA
Power Consumption per end	540	mW	Nominal Power
Electrical Interface and Pin-out	38-pin edge connector		Pin-out as defined by the QSFP+ MSA

III. Optical Characteristics

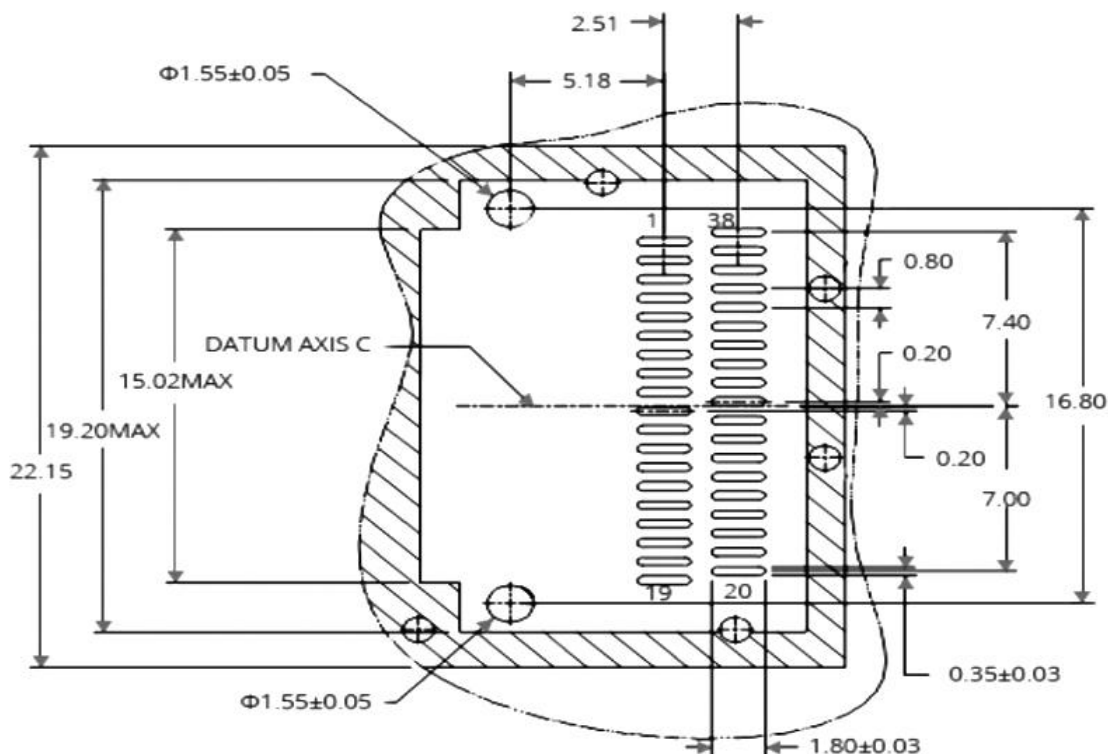| Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Transmitter						
Center Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.65	nm	-
Average launch power, each lane	Pout	-7.5	-	2.5	dBm	-
Difference in launch power between any two lanes (OMA)				4	dB	-
Extinction Ratio	ER	3	-	-	dB	-
Peak power, each lane				4	dBm	-
Transmigrate and dispersion penalty (TDP), each lane	TDP			3.5	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4				Hit Ratio = 5x10-5
Receiver						
Center Wavelength	λc	840	850	860	nm	-
Stressed receiver sensitivity in OMA, each lane				-5.4	dBm	1
Maximum Average power at receiver input, each lane				2.4	dBm	-
Receiver Reflectance				-12	dB	-
Peak power, each lane				4	dBm	-
LOS Assert		-30			dBm	-
LOS De-Assert – OMA				-7.5	dBm	-
LOS Hysteresis		0.5			dB	-

Note:

1.Measured with conformance test signal at TP3 for BER = 10e-12

IV. Pin Description

QSFP+ Module Pad Layout (Top View)

	Top Side		Bottom Side	
38	GND		GND	1
37	TX1n		TX2n	2
36	TX1p		TX2p	3
35	GND		GND	4
34	TX3n		TX4n	5
33	TX3p		TX4p	6
32	GND		GND	7
31	LPMode		ModselL	8
30	Vcc1		ResetL	9
29	VccTx		VccRx	10
28	IntL		SCL	11
27	ModPrsL		SDA	12
26	GND		GND	13
25	RX4p		RX3p	14
24	RX4n		RX3n	15
23	GND		GND	16
22	RX2p		RX1p	17
21	RX2n		RX1n	18
20	GND		GND	19

Module Card Edge

Top Side Viewed From Top

Bottom Side Viewed From Bottom

Host PCB Layout (Top View)

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	2
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	2
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1

20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	2
28	LVTTL-O	IntL	Interrupt	2
29		Vcc Tx	+3.3V Power Supply Transmitter	
30		Vcc1	+3.3V Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Notes:

1.Module ground pins GND are isolated from the module case and chassis ground within the module.

2.Shall be pulled up with 4.7K-10Kohms to a voltage between 3.14V and 3.47V on the host board.

V. Low Speed Electrical Hardware Pins

In addition to 2-wire serial interface, 40G QSFP+ AOC module has the following low speed pins for control and status:

(1) ModPrsL

ModPrsL is an output pin. When "low", indicates the module is present. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

(2) IntL

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The source of the interrupt could be identified by using the 2-wire serial interface.

(3) LPMode

LPMode is a control pin. When "High", it could be used to set the module in low power mode (<1.5W). This pin, along with Power_overide bit and Power_set bit in management interface could be used to avoid system power crash. 40G QSFP+ AOC, however consumes less than 1.5W. Therefore this pin takes no effect.

(4) ModSelL

ModSelL is an input signal. When held low by the host, the module responds to two-wire serial communication commands. The ModSelL signal allows multiple QSFP modules to be on a single two-wire interface bus. When the ModSelL signal is "High", the module will not respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input pin is biased to a "High" state in the module.

In order to avoid conflicts, the host system must not attempt two-wire interface communications within the ModSelL deassert time after any QSFP modules are de-selected. Similarly, the host must wait for the period of the ModSelL assert time before communicating with the newly selected module. The assert and deassert periods of different modules may overlap as long as the above timing requirements are met.
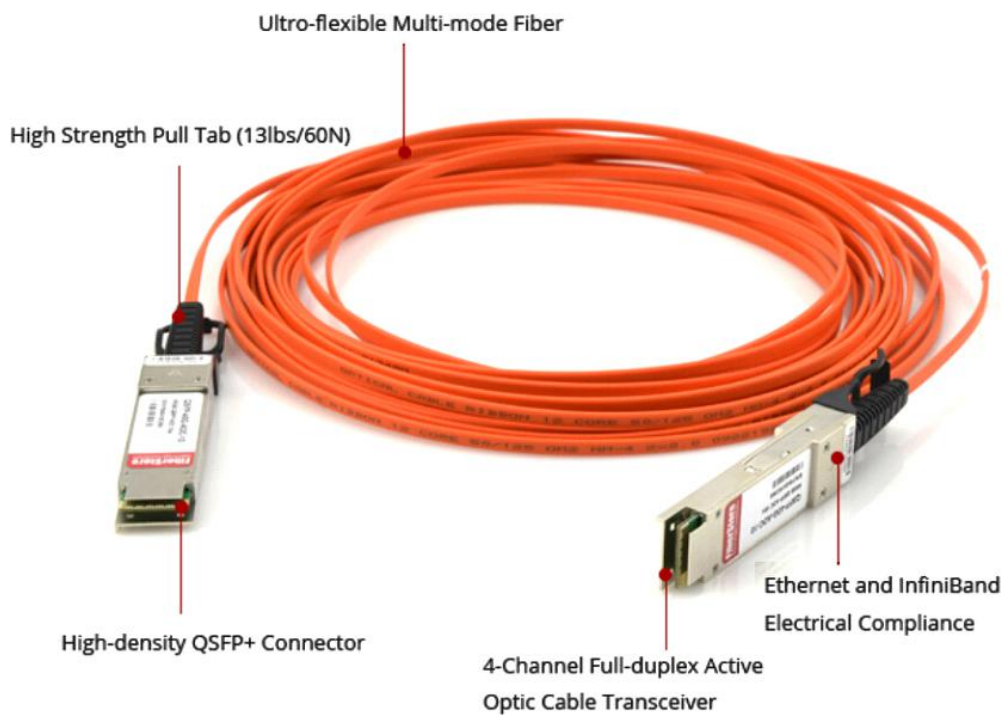
(5) ResetL

The ResetL signal is pulled to Vcc in the QSFP+ module. A logic low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host will disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power-up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.
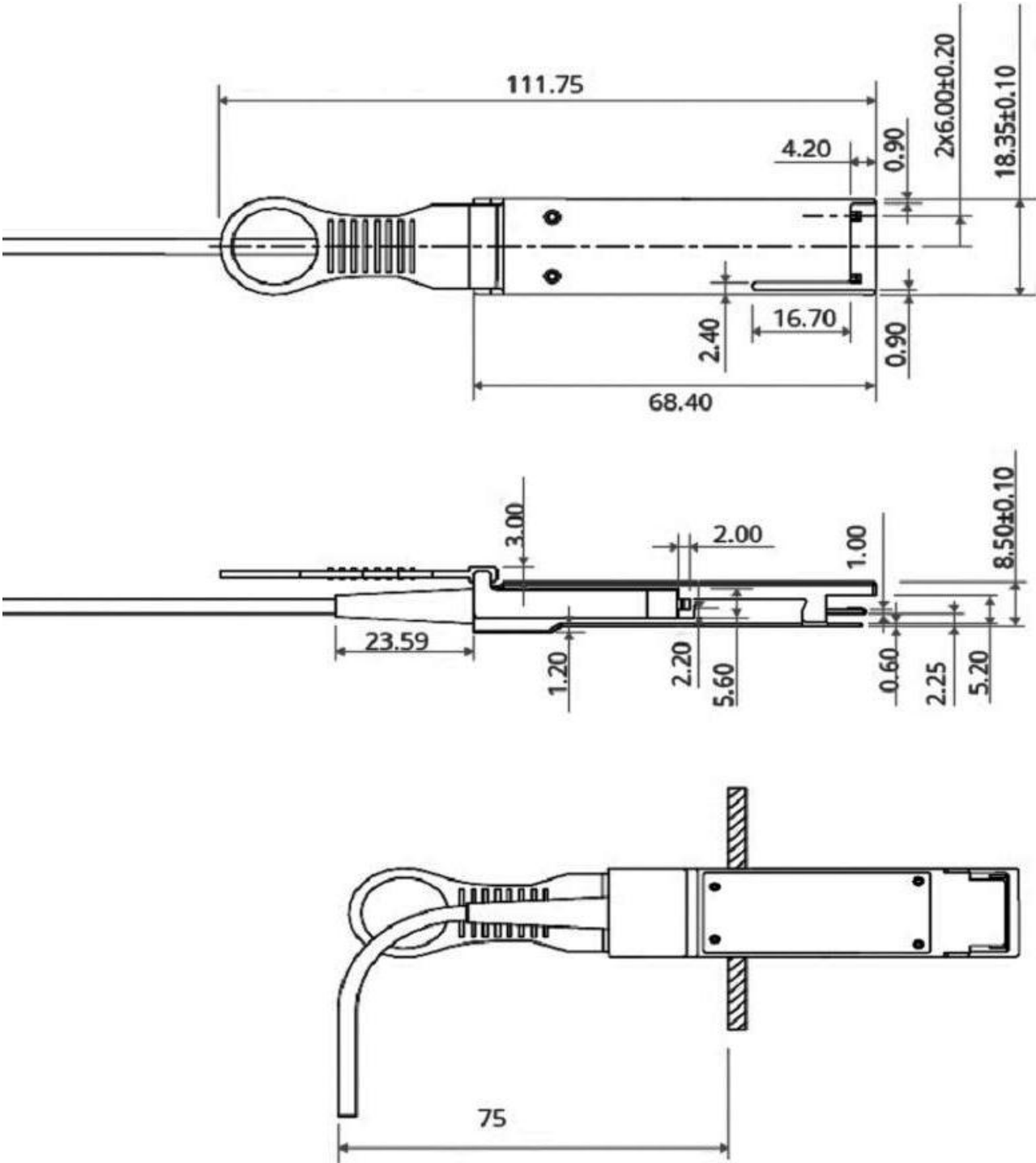
VII. Module Block Diagram
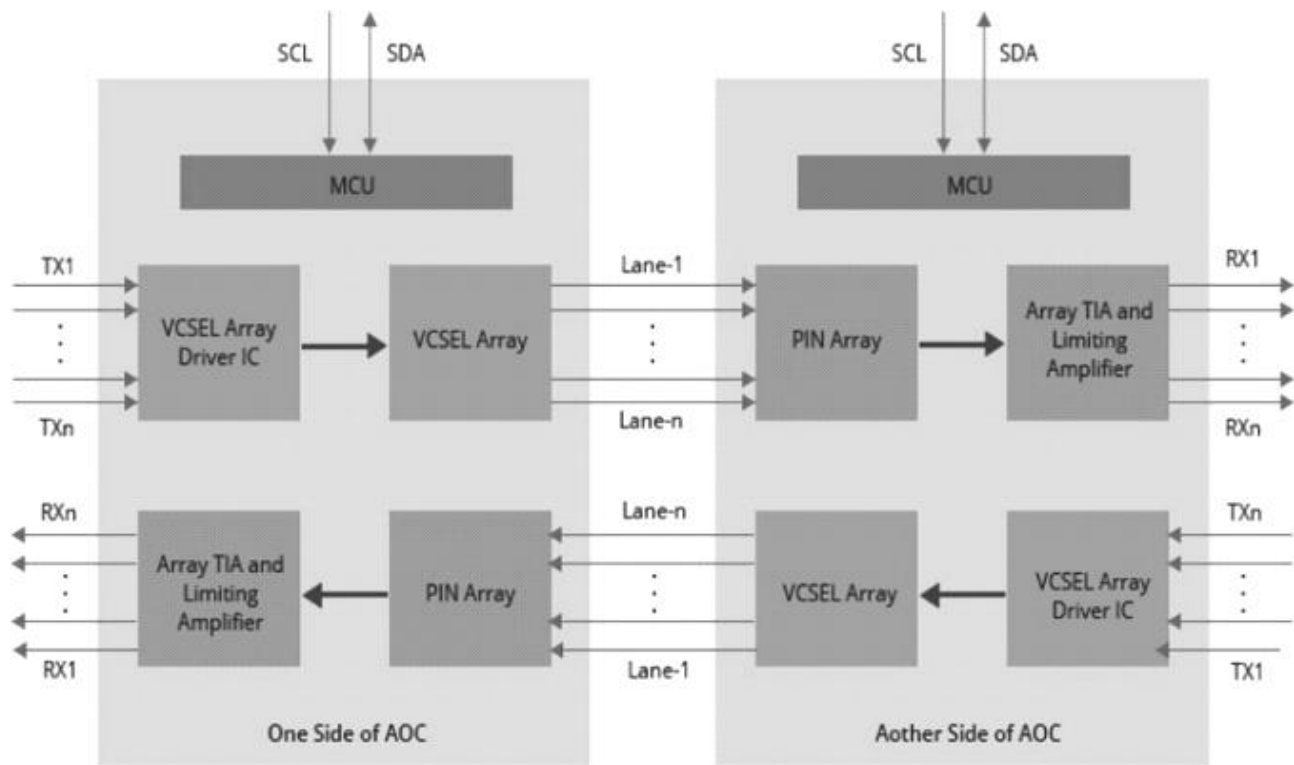
AOC is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I2C system can contact with module.

Ultro-flexible Multi-mode Fiber

High Strength Pull Tab (13lbs/60N)

High-density QSFP+ Connector

4-Channel Full-duplex Active Optic Cable Transceiver

Ethernet and InfiniBand Electrical Compliance

VIII. Mechanical Outline Dimensions

XI. Installation

Caution:

Follow accepted ESD practices when handling QSFP+ connectors to prevent damage to the internal components within the connector. ESD (electrostatic discharge) is the sudden flow of electricity between two objects at different voltage potentials caused by contact. The basis of any ESD protection strategy is to ground or bring all elements in the ESD protected area to the same potential. An ESD wrist strap should be used for everything in the ESD protected area including personnel, tools, cabinets and components.

A. Installing QSFP+ Modules

Follow these steps to install a FS.COM QSFP+ cable assembly:

Step 1.   Remove the protective ESD cap from the connector.

Step 2.   Slide the QSFP+ cable end into the slot until it locks into position (see figure 1).

There is an audible click when the connector is properly seated.

Figure 1. Installing an QSFP+ Module	Figure 2. Disconnecting Latch Mechanism	Figure 3. Removing Modules

Caution :

The latching mechanism locks the QSFP+ connector into place when cables are connected. Do not pull on the cable in an attempt to remove the QSFP+ connector.

B. Removing QSFP+ Modules

Follow these steps to remove a FS.COM QSFP+ cable assembly:

Step 1.   Pull on the QSFP+ latch pull lanyard. See figure 2.

Step 2.   Grasp the QSFP+ connector on both sides and remove it from the system. See figure 3.

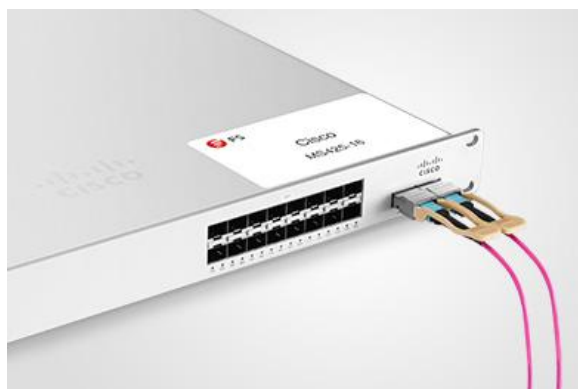Step 3.   If possible, replace the ESD protective cap or put the QSFP+ into an ESD protected bag.

Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.

Cisco Catalyst C9500-24Y4C

Cisco MS425-16

Brocade VDX 6940-144S


Dell EMC Networking Z9100-ON

Force⑩tm S60-44T

HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.
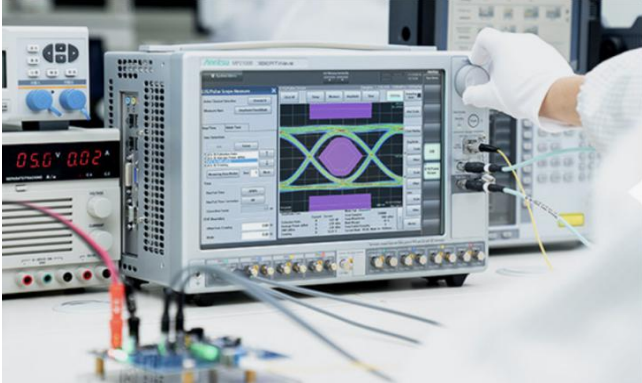
1. TX/RX Single Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator the input and output signal quality.

- Eye Pattern Measurements: Jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0℃ to 70℃
- Extended: -5℃ to 85℃
- Industrial: -40℃ to 85℃

3. Transfer Rate and Protocol Testing

Test the actual transfer data rate and the transmission ability under different protocols with Networks Master Pro.

- Ethernet
- Fiber Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width
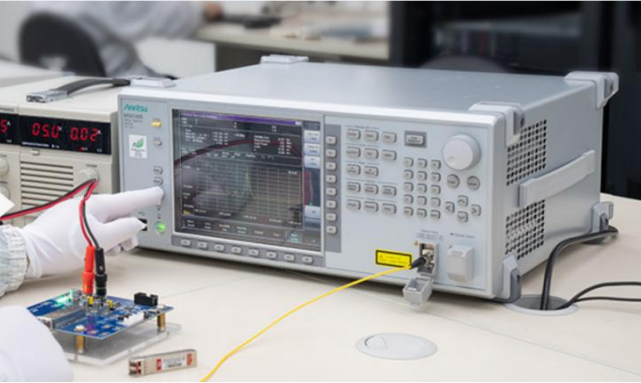
Order Information

Part Number	Data Rate	Length	Connector Type	Temp. Range	Cable Jacket
QSFP-AO01	Up to 40G	1m	QSFP+ AOC	0-70℃	ONFP
QSFP-AO02	Up to 40G	2m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO03	Up to 40G	3m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO05	Up to 40G	5m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO07	Up to 40G	7m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO10	Up to 40G	10m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO15	Up to 40G	15m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO20	Up to 40G	20m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO25	Up to 40G	25m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO30	Up to 40G	30m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO50	Up to 40G	50m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO75	Up to 40G	75m	QSFP+ AOC	0-70℃	OFNP
QSFP-AO100	Up to 40G	100m	QSFP+ AOC	0-70℃	OFNP

Notes:

1.40G QSFP+ AOC is individually tested on corresponding equipment such as Cisco, Arista, Juniper, Dell, Brocade and
other brands, and passes the monitoring of FS.COM intelligent quality control system.

2.Customized 40G QSFP+ AOCs are available in various lengths.

United Kingdom
Russia
Germany
United States
China
Singapore
Australia

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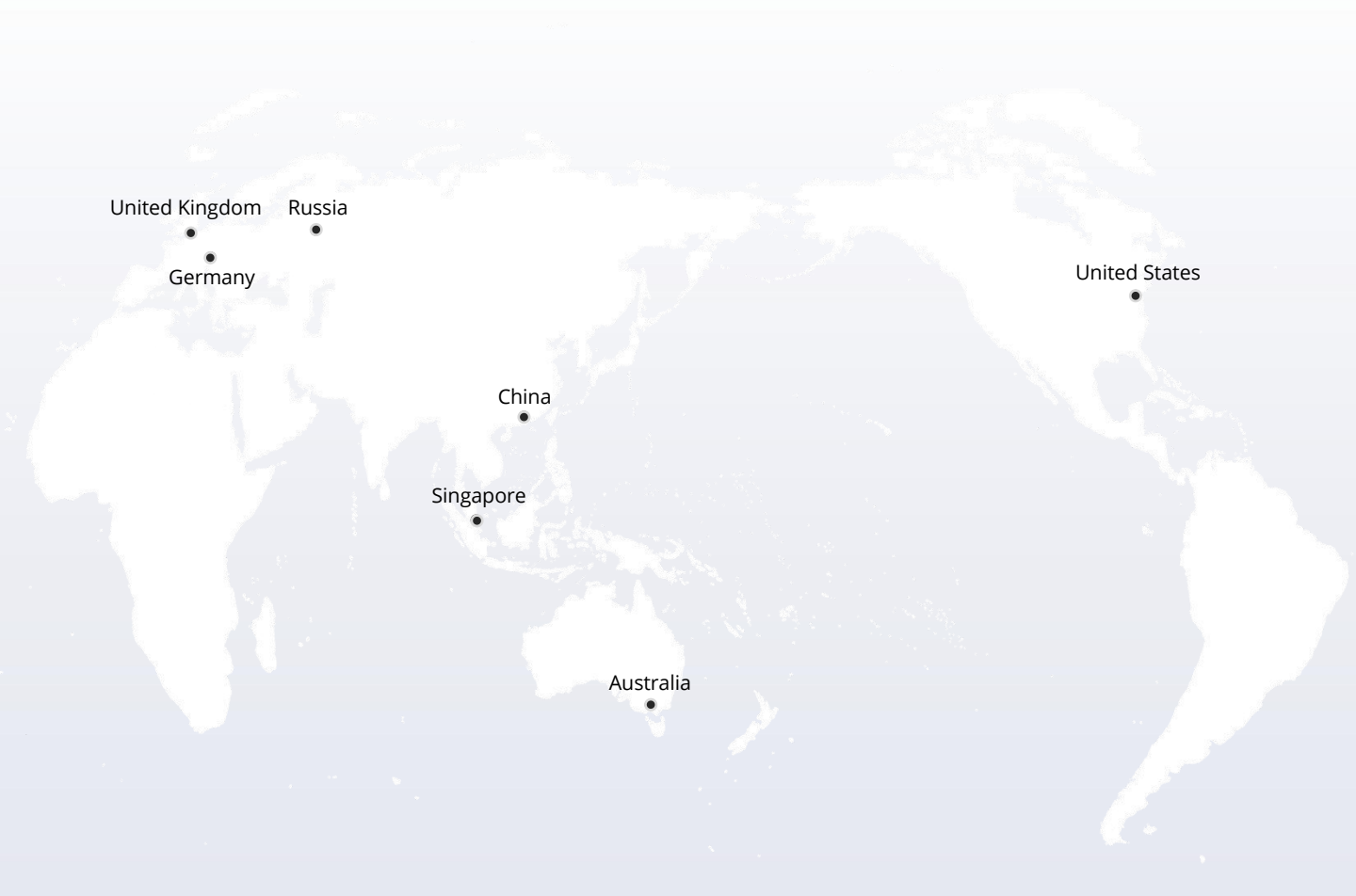
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