

400G QSFP-DD to 4 x100G QSFP28 Active Direct Attach Copper Breakout Cable



Application

- 400G to 4x100G Ethernet

Features

- Recognizable, purple PVC jacket
- 400G to 4x100G with gearbox function
- CMIS compliant (QSFP-DD end)
- SFF-8636 compliant (QSFP28 end)
- Single 3.3V power supply
- Low power consumption:
 - QSFP-DD end: Typ. 8.5W
 - QSFP28 end: Typ. 3.5W
- BER < 10^{-15} (post FEC)
- Hot pluggable
- RoHS2 compliant
- I²C management interface
- Operating case temperature range: 0 to +70°C

Description

400G QSFP-DD to 4 x100G QSFP28 Active Direct Attach Copper Breakout Cable (Active Electrical Cable) enables low-power, high-reliability and high-speed interconnections over very thin copper cables without using any optical components.

The product is designed for hyper-scale data center use. The 400G cable breaks out from one 400G (8x53G-PAM4) QSFP-DD end into four 100G (4x25G-NRZ) QSFP28 ends with built-in gearbox feature. The use and replacement of 400G QSFP-DD to 4x100G QSFP28 Active Direct Attach Copper Breakout Cable (Active Electrical Cable) is simple and straightforward as it adopts standard QSFP-DD type 2/QSFP28 form factors and complies to MSA specifications.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltage	-0.3	3.465	V
Data Input Voltage	0	1.8	V
Control Input Voltage	-0.3	3.6	V
Storage Temperature Range	-10	+85	°C
Operating Case Temperature Range	0	+70	°C
Operating Relative Humidity	0	80	%

II. General Product Characteristics

Parameter	Value	Comments
Module Form Factor	QSFP-DD and QSFP28	
Number of Data Lanes	8 TX and 8 RX per Module (PAM4)	QSFP-DD
	4 TX and 4 RX per Module (NRZ)	QSFP28
Maximum Aggregate Data Rate	400Gbps	
Nominal Data Rate per Lane	53.125Gbps (PAM4)	QSFP-DD
	25.78125Gbps (NRZ)	QSFP28
Electrical Interface and Pin-out	76-Pin edge Connector	QSFP-DD
	38-Pin edge Connector	QSFP28
Pin Description	Per QSFP-DD Hardware Specification (QSFP-DD) and per SFF-8679 (QSFP28)	
Management Interface	I2C, Serial, Timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers	QSFP-DD
	I2C, Serial, Timing per SFF-8636	QSFP28
Length of AEC	1, 3, 5	Meters, Using Copper
BER (Pre-FEC)	$<10^{-8}$	Tested with QPRBS31 Pattern
BER (Post-FEC)	$<10^{-15}$	Tested with QPRBS31 Pattern
Power Supply (DC)	3.3V	

III. Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption @QSFP-DD			8.5		W
Power Consumption @QSFP28			3.5		W
Supply Voltage, VccTx, VccRx		3.135	3.3	3.465	VDC
Supply Current, Icc@QSFP-DD			2570		mA
Supply Current, Icc@QSFP28			1050		mA
Power Supply Noise Tolerance			25		mVpp

Active Cable Input Electrical Characteristics per Lane

Input Differential Voltage			Complies with Standards		
Signaling Rate/Channel @QSFP-DD	PAM4		53.125 25.78125		Gb/s
Signaling Rate/Channel @QSFP28	NRZ		25.78125		Gb/s
RX Input Resistance		90	100	ohms	110
Input Jitter Tolerance			Complies with Standards		
Input Common Mode Noise				10	mV-rms

IV. ESD Ratings

ESD Standard	Level	Maximum Rating		Units
		Contact Discharge	Air Discharge	
IEC/EN6100-4-2	4	±8k	±15k	V

Parameter	Conditions	Min.	Typ.	Max.	Units
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Active Cable Output Electrical Characteristics per Lane

Output Equalization Coefficient Step Size		1.5		5	%
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Output Total Jitter

Complies with standards

TX Output Impedance		80	100	120	oh ms
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Latency Characteristics

Total Latency				160	ns
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V. Module Output Characteristics (atTP4*)

Notes: *Please refer to IEEE802.3bs 120E and IEEE802.3bm 83E for TP4 definition.

QSFP-DD End

Parameter	Value	Units
Signaling Rate Per Lane (Range)	26.5625±100 ppm	GBd
AC Common-mode Output Voltage (Max, RMS)	17.5	mV
Differential Peak-to-Peak Output Voltage (Max.)	900	mV
Near-End ESMW (Eye Symmetry Mask Width)	0.265	UI
Near-End Eye Height, Differential (Min.)	70	mV
Far-End ESMW (Eye Symmetry Mask Width)	0.2	UI
Far-End Eye Height, Differential (Min.)	30	mV

Parameter	Value	Units
Transition Time (Min. 20% to 80%)	9.5	ps
DC Common Mode Voltage (Min.)^a	-350	mV
DC Common Mode Voltage (Max.)^a	2850	mV

A DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

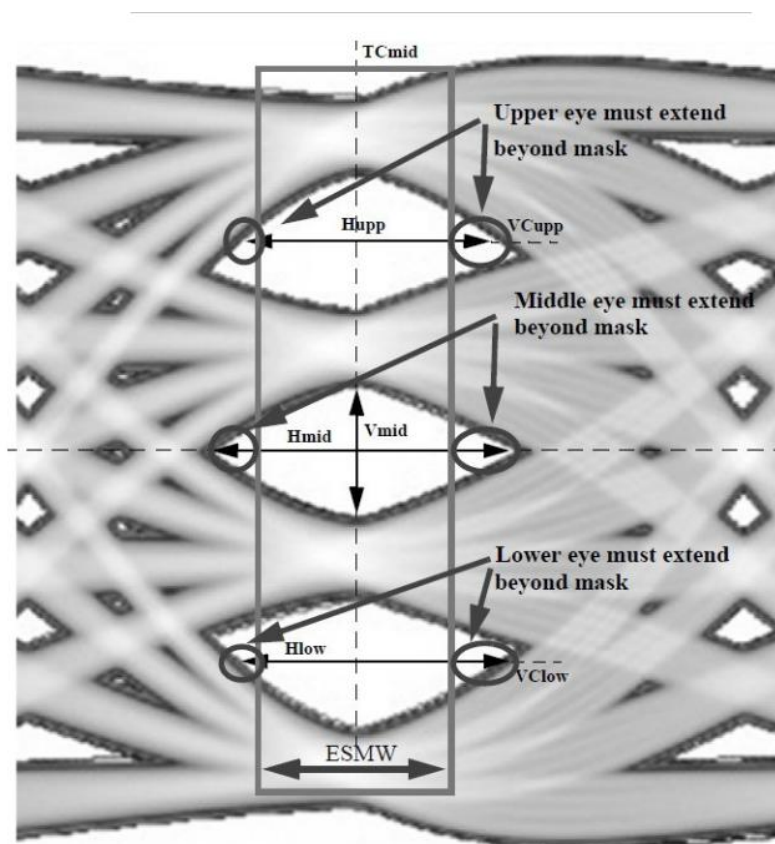


Figure 6-1 PAM4 Upper, Middle, and Lower Eye Mask

QSFP28 End

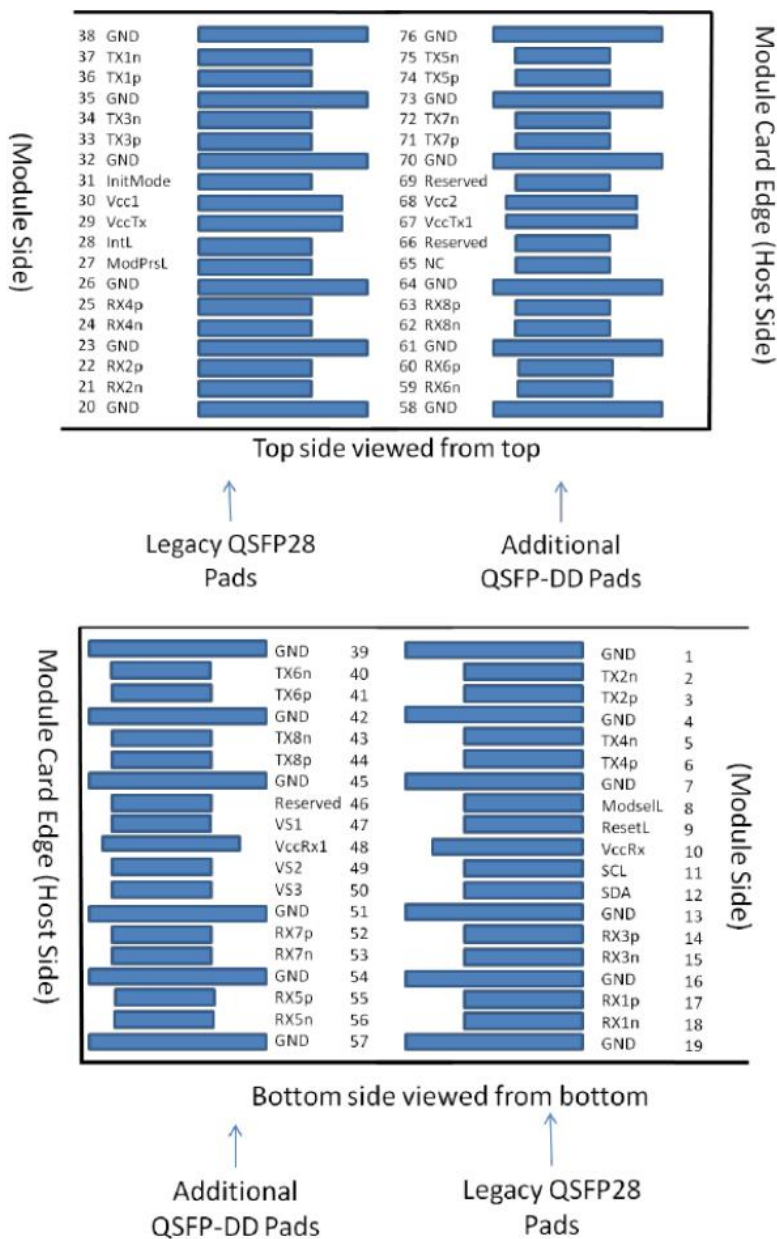
Parameter	Value	Units
Signaling Rate per Lane (Range)	25.78125±100ppm	GBd
AC Common-Mode Output Voltage (Max, RMS)	17.5	mV
Differential Output Voltage (Max.)	900	mV
Eyewidth (Min.)	0.57	UI
Eyeheight, Differential (Min.)	228	mV
Transition Time (Min. 20% to 80%)	12	ps
DC Common Mode Voltage (Min.)^a	-350	mV
DC Common Mode Voltage (Max.)^a	2850	mV

A DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

VI. Pin Description

QSFP28 End

Figure 7-1 QSFP-DD MSA-compliant 76-pin Connector



Pin	Symbol	Description
1	GND	Ground
2	Tx2n	Transmitter Inverted Data Input
3	Tx2p	Transmitter Non-Inverted Data Input
4	GND	Ground
5	Tx4n	Transmitter Inverted Data Input
6	Tx4p	Transmitter Non-Inverted Data Input
7	GND	Ground
8	ModSelL	Module Select
9	ResetL	Module Reset
10	V _{cc} Rx	+3.3V Power Supply Receiver
11	SCL	2-wireserial Interface Clock
12	SDA	2-wireserial Interface Data
13	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output
15	Rx3n	Receiver Inverted Data Output
16	GND	Ground

Pin	Symbol	Description
17	Rx1p	Receiver Non-Inverted Data Output
18	Rx1n	Receiver Inverted Data Output
19	GND	Ground
20	GND	Ground
21	Rx2n	Receiver Inverted Data Output
22	Rx2p	Receiver Non-Inverted Data Output
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output
25	Rx4p	Receiver Non-Inverted Data Output
26	GND	Ground
27	ModPrsL	Module Present
27	ModPrsL	Module Present
28	IntL	Interrupt
29	V _{cc} Tx	+3.3V Power Supply Transmitter
30	V _{cc} 1	+3.3V Power Supply
31	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE

Pin	Symbol	Description
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input
38	GND	Ground
39	GND	Ground
40	Tx6n	Transmitter Inverted Data Input
41	Tx6p	Transmitter Non-Inverted Data Input
42	GND	Ground
43	Tx4n	Transmitter Inverted Data Input
44	Tx4p	Transmitter Non-Inverted Data Input
45	GND	Ground
46	Reserved	For Future Use

Pin	Symbol	Description
47	VS1	Module Vendor Specific 1
48	V _{cc} Rx1	3.3V Power Supply
49	VS2	Module Vendor Specific 2
50	VS3	Module Vendor Specific 3
51	GND	Ground
52	Rx7p	Receiver Non-Inverted Data Output
53	Rx7n	Receiver Inverted Data Output
54	GND	Ground
55	Rx5p	Receiver Non-Inverted Data Output
56	Rx5n	Receiver Inverted Data Output
57	GND	Ground
58	GND	Ground
59	Rx6n	Receiver Inverted Data Output
60	Rx6p	Receiver Non-Inverted Data Output
61	GND	Ground

Pin	Symbol	Description
62	Rx8n	Receiver Inverted Data Output
67	V _{cc} T1x	3.3V Power Supply
68	V _{cc} 2	3.3V Power Supply
69	Reserved	For Future Use
70	GND	Ground
71	Tx7p	Transmitter Non-Inverted Data Input
72	Tx7n	Transmitter Inverted Data Input
73	GND	Ground
74	Tx5p	Transmitter Non-Inverted Data Input
75	Tx5n	Transmitter Inverted Data Input
76	GND	Ground

QSFP28 End

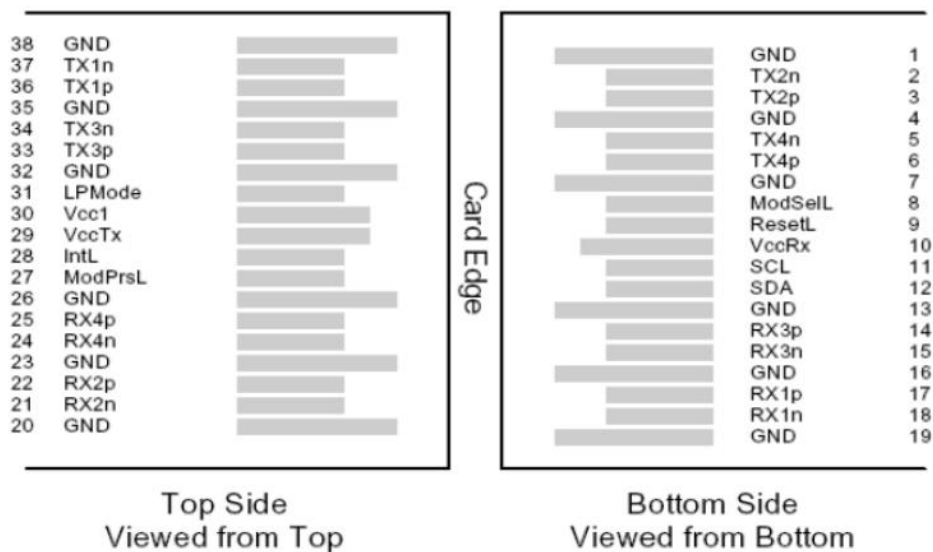


Figure 7-2 QSFP-compliant 38-pin Connector (per SFF-8679)

Pin	Symbol	Description
1	GND	Ground
2	Tx2n	Transmitter Inverted Data Input
3	Tx2p	Transmitter Non-Inverted Data Input
4	GND	Ground
5	Tx4n	Transmitter Inverted Data Input
6	Tx4p	Transmitter Non-Inverted Data Input

Pin	Symbol	Description
7	GND	Ground
8	ModSelL	Module Select
9	ResetL	Module Reset
10	V _{cc} Rx	+3.3V Power Supply Receiver
11	SCL	2-Wireserial Interface Clock
12	SDA	2-Wireserial Interface Data
13	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output
15	Rx3n	Receiver Inverted Data Output
16	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output
18	Rx1n	Receiver Inverted Data Output
19	GND	Ground
20	GND	Ground

Pin	Symbol	Description
21	Rx2n	Receiver Inverted Data Output
22	Rx2p	Receiver Non-Inverted Data Output
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output
25	Rx4p	Receiver Non-Inverted Data Output
26	GND	Ground
27	ModPrsL	Module Present
28	IntL	Interrupt
29	V _{cc} Tx	+3.3V Power Supply Transmitter
30	V _{cc} 1	+3.3V Power Supply
31	LPMode	Low Power Mode
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input

Pin	Symbol	Description
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input
38	GND	Ground

VII. Mechanical Cable Characteristics

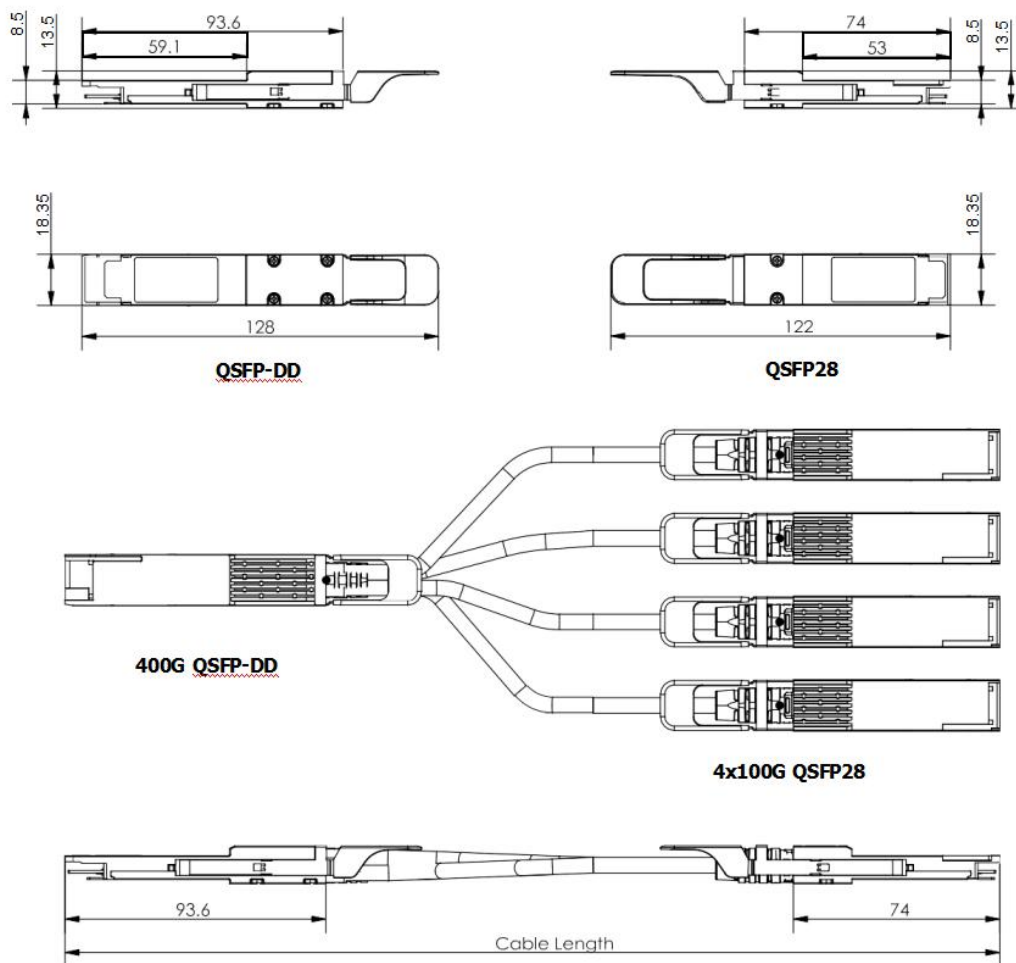


Figure 8-1 Mechanical Dimensions (Unit: mm)

Materials

- Zinc alloy die casting shells with Ni plated & latching mechanism parts.
- High-speed data connection cable with EMI shielding braid and PVC jacket.
- Thermo plastic latch pull tab.

VIII. Cable Mechanical Specifications

Parameter	Types	Min.	Typ.	Max.	Units
Diameter	4P 30AWG	5.0	5.3	5.6	mm
QSFP-DD End					
Minimum Bend Radius	4P 30AWG × 4		26.5		mm
Minimum Bend Space	4P 30AWG × 4		73		mm
QSFP28 End					
Minimum Bend Radius	4P 30AWG		26.5		mm
Minimum Bend Space	4P 30AWG		54		mm

IX. Insertion, Extraction and Retention Forces

Parameter	Min.	Max.	Units	Note
Insertion				
QSFP-DD Module	0	90	N	
QSFP28 Module	0	40	N	
Extraction				
QSFP-DD Module	0	50	N	
QSFP28 Module	0	30	N	
Retention				
QSFP-DD Module	90	N/A	N	No Damage to Module Below 90N With Latch Engaged
QSFP28 Module	90	N/A	N	No Damage to Module Below 90N With Latch Engaged
Insertion/Removal Cycles				
QSFP-DD Module	50	N/A	Cycles	Number of Cycles for an Individual Module
QSFP28 Module	50	N/A	Cycles	Number of Cycles for an Individual Module

Memory Map

QSFP-DD end: Compatible with Common Management Interface Specification for 8X/16X Pluggable Transceivers.

QSFP28 end: Compatible with SFF-8636.

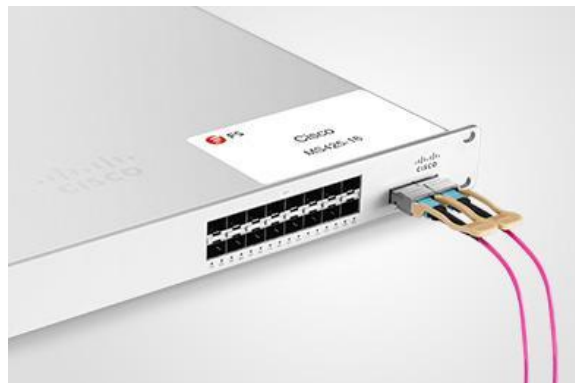
Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.



Cisco Catalyst C9500-24Y4C



Cisco MS425-16



Brocade VDX 6940-144S



Dell EMC Networking Z9100-ON



Force@tm S60-44T

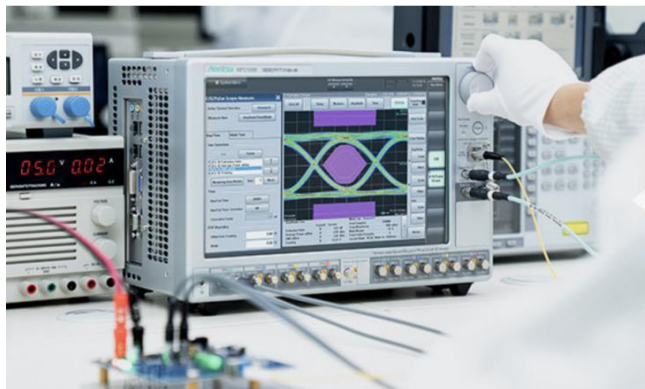


HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the [Test Bed](#) PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Signal Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator to ensure the input and output signal quality.

- Eye Pattern Measurements: jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic changes in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0 °C to 70 °C
- Extended: -5 °C to 85 °C
- Industrial: -40 °C to 85 °C



3. Transfer Rate and Protocol Testing

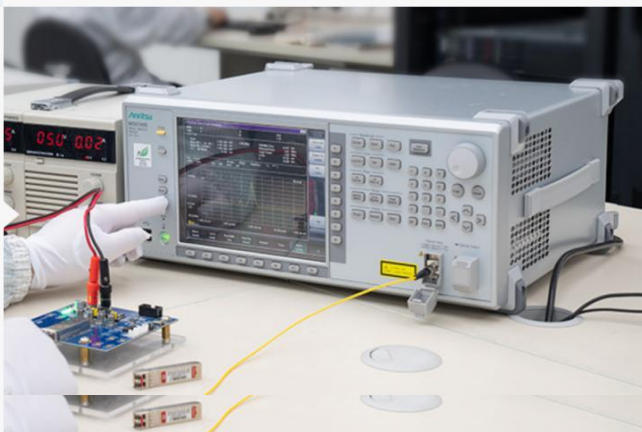
Test the actual transfer data rate and the transmission ability under different protocols with Network Master Pro.

- Ethernet
- Fibre Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

Part Number	Data Rate	Length	Wire Gauge	Connector Type	Temp. Range	Cable Jacket
Q-4S28PC01	Up to 400G	1m	AWG30	Active Copper	0-70°C	PVC
Q-4S28PC03	Up to 400G	3m	AWG30	Active Copper	0-70°C	PVC
Q-4S28PC05	Up to 400G	5m	AWG30	Active Copper	0-70°C	PVC



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