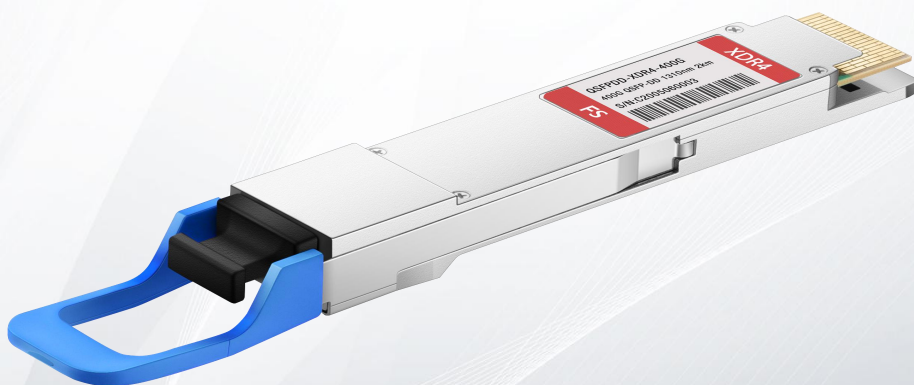# QSFP-DD 400GBASE-DR4+ 1310nm 2km Transceiver

QSFPDD-XDR4-400G

Application

- 400G Ethernet
- Infiniband Interconnect
- Datacenter Enterprise Networking

Features

- Compliant to QSFP-DD MSA
- Parallel 4 Optical Lanes
- 100G Lambda MSA 100G-FR Specification compliant
- Up to 2km transmission on single mode fiber (SMF) with FEC
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel
- Case temperature range: 0 ~ +70℃
- Maximum power consumption 12W
- MPO-12 connector
- RoHS complaint

General Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP-DD DR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP-DD MSA-compliant edge type connector.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

The module incorporates 4 parallel channels on 1310nm center wavelength, operating at 100G per channel. The transmitter path incorporates a quad channel EML driver together with 4 parallel EMLs. On the receiver path, a PD array is connected with a quad channel TIA to convert the parallel 400Gb/s optical input into 4 channels of parallel 100Gb/s (PAM4) electrical signals. A DSP basis gearbox is used to convert 8 channels of 25GBaud PAM4 signals into 4 channels of 50GBaud PAM4 signals and also an 8-channel retimer and FEC block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to QSFP-DD MSA with MPO-12 connector.

A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Initialize Mode (InitMode) is an input signal. It is pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Product Specifications

I. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Storage Temperature	Ts	-40		85	℃	
Operating Case Temperature	T_{OP}	0		70	℃	
Power Supply Voltage	Vcc	-0.5		3.6	V	
Relative Humidity (non-condensation)	RH	0		85	%	
Damage Threshold, each Lane	TH_d	5.5			dBm	

II. Recommended Operating Environment

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Operating Case Temperature	T_{op}	0		70	℃	
Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4×10^{-4}		
Post-FEC Bit Error Ratio				1×10^{-12}		1
Link Distance	D	0.002		2	km	2

Notes:

1. FEC provided by host system.

2. FEC required on host system to support maximum distance.

III. Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Center Wavelength	λc	1304.5	1310	1317.5	nm	
Transmitter						
Modulation Format			PAM4			
Data Rate, each lane			53.125 ± 100 ppm		GBd	
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each lane	P_{AVG}	-2.4		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA$_{outer}$), each lane	P_{OMA}	-0.2		4.2	dBm	2
Launch Power in OMA$_{outer}$ minus TDECQ, each Lane for ER ≥ 5dB for ER < 5dB		-1.6 -1.5			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
TDECQ – $10*\log_{10}$(Ceq), each Lane				3.4	dB	3
Extinction Ratio	ER	3.5			dB	
RIN$_{21.4}$OMA	RIN			-136	dB/HZ	
Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	R_T			-26	dB	
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	

Receiver						
Modulation Format			PAM4			
Data Rate, each lane			53.125 ± 100 ppm		GBd	
Damage Threshold, each Lane	TH_d	5.5			dBm	4
Average Receive Power, each Lane		-6.4		4.5	dBm	5
Receive Power (OMA$_{outer}$), each Lane				4.7	dB	
Receiver Sensitivity (OMA$_{outer}$), each Lane	SEN			Equation (1)	dBm	6
Stressed Receiver Sensitivity (OMA$_{outer}$), each Lane	SRS			-2.5	dBm	7
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-15			dBm	
LOS De-assert	LOSD			-9.4	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 8)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
SECQ – 10*log$_{10}$(Ceq), Lane under Test				3.4	dB	
OMA$_{outer}$ of each Aggressor Lane			4.7		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 5 dB, the OMAouter (min) must exceed the minimum value specified here.

3. C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

6. Receiver sensitivity (OMA$_{outer}$), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation (1), which is illustrated in Figure 4.

$$RS = \max(-4.5, SECQ - 5.9) \text{ dBm} \qquad (1)$$

Where:
RS   is the receiver sensitivity, and
SECQ   is the SECQ of the transmitter used to measure the receiver sensitivity.

7. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}.

8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
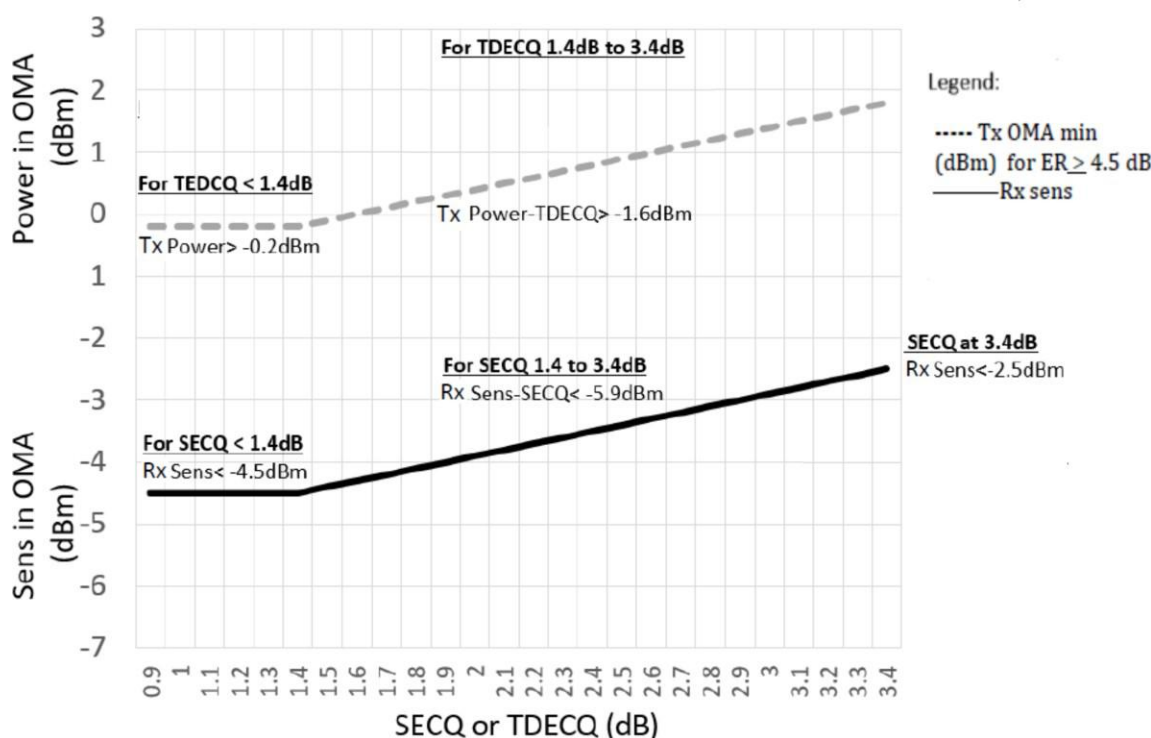

Figure 1. Illustration of Receiver Sensitivity Mask for 400G-DR4+

IV. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typ.	Max	Unit	Ref.
Power Consumption				12	W	
Supply Current	Icc			3.64	A	
Transmitter (each lane)						
Signaling Rate, each Lane	TP1		26.5625±100 ppm		GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each lane)						
Signaling Rate, each Lane	TP4		26.5625±100 ppm		GBd	
Differential pk-pk Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				

Parameter						
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

2. Meets BER specified in IEEE 802.3bs 120E.1.1.

3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

V. Digital Diagnostic Monitoring Information

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Unit	Ref.
Temperature Monitor Absolute Error	DMI_Temp	-3	3	℃	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

VI. Pin Assignment

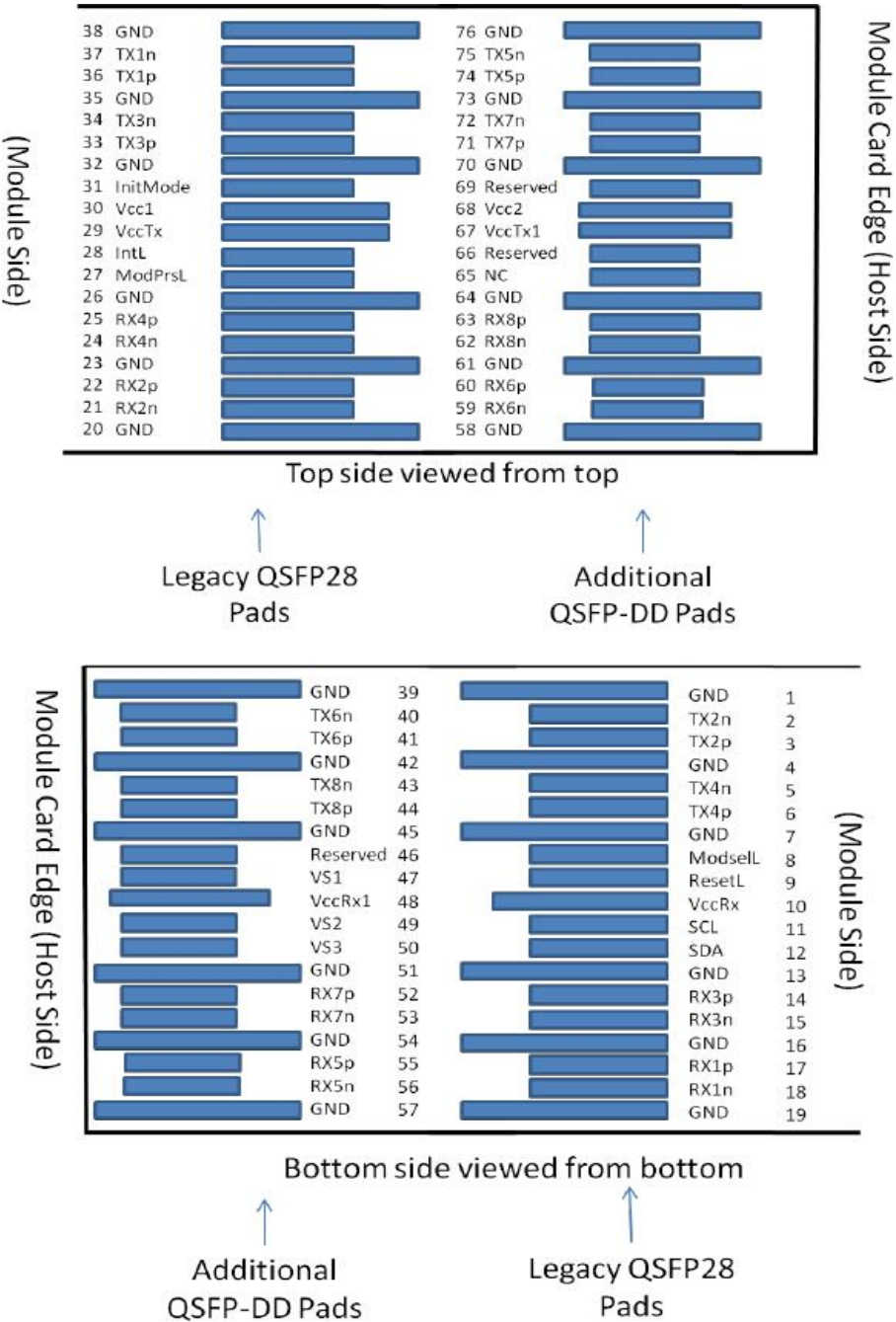The electrical pinout of the QSFP-DD module is shown in Figure 2 below.

Figure 2. MSA Compliant Connector

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	

26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2

49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reseved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reseved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output	3A	

72	CML-I	Tx7n	Transmitter Inverted Data Output	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Output	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 Kohms and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.
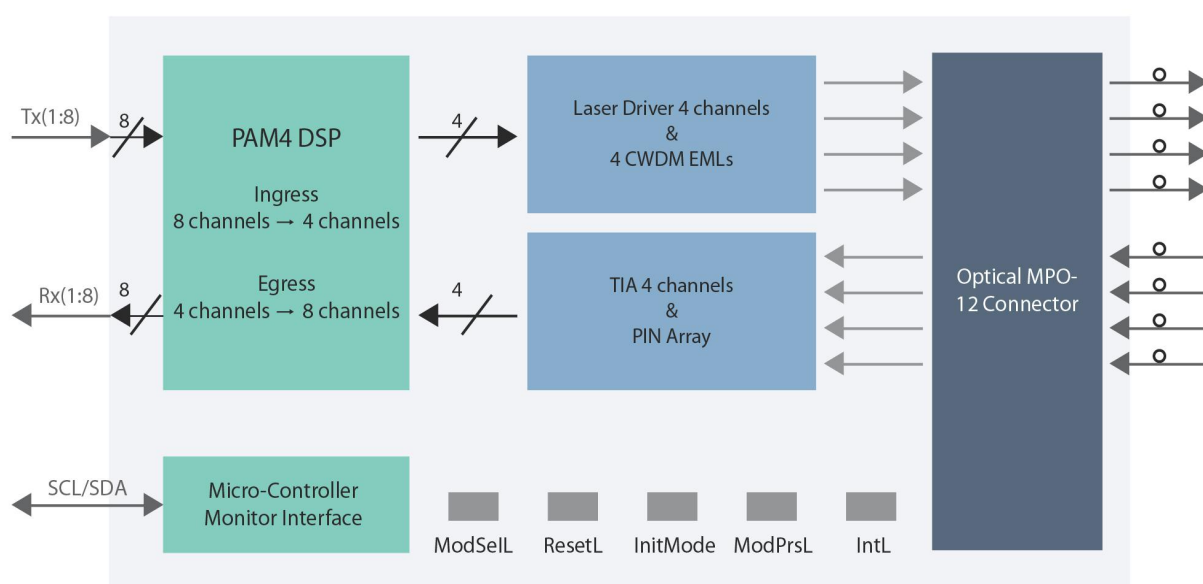
VII. Optical Module Block Diagram

Figure 3. Transceiver Block Diagram
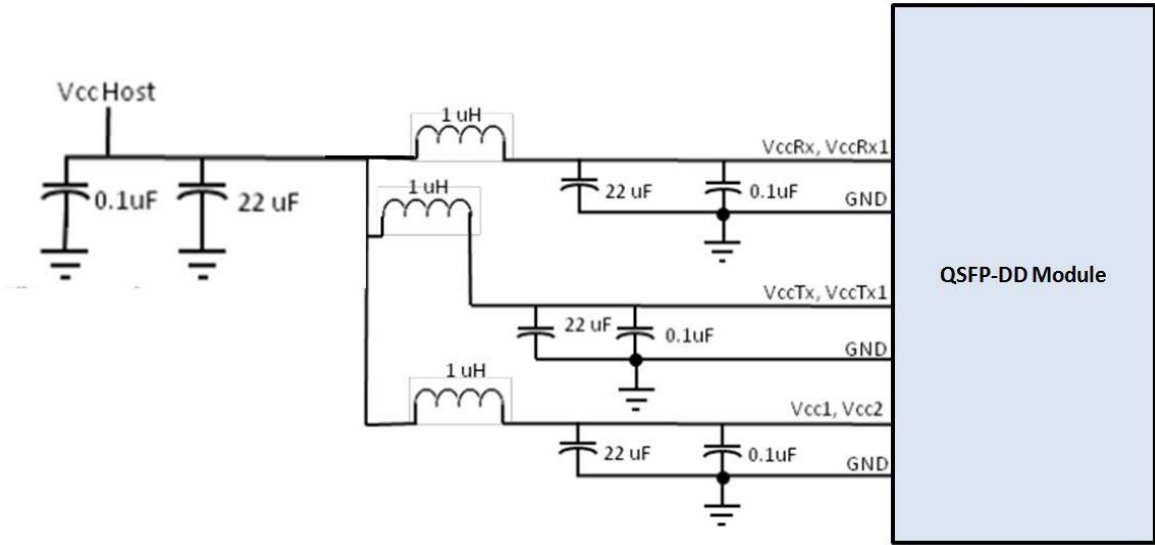
VIII. Recommended Power Supply Filter

Figure 4. Recommended Power Supply Filter

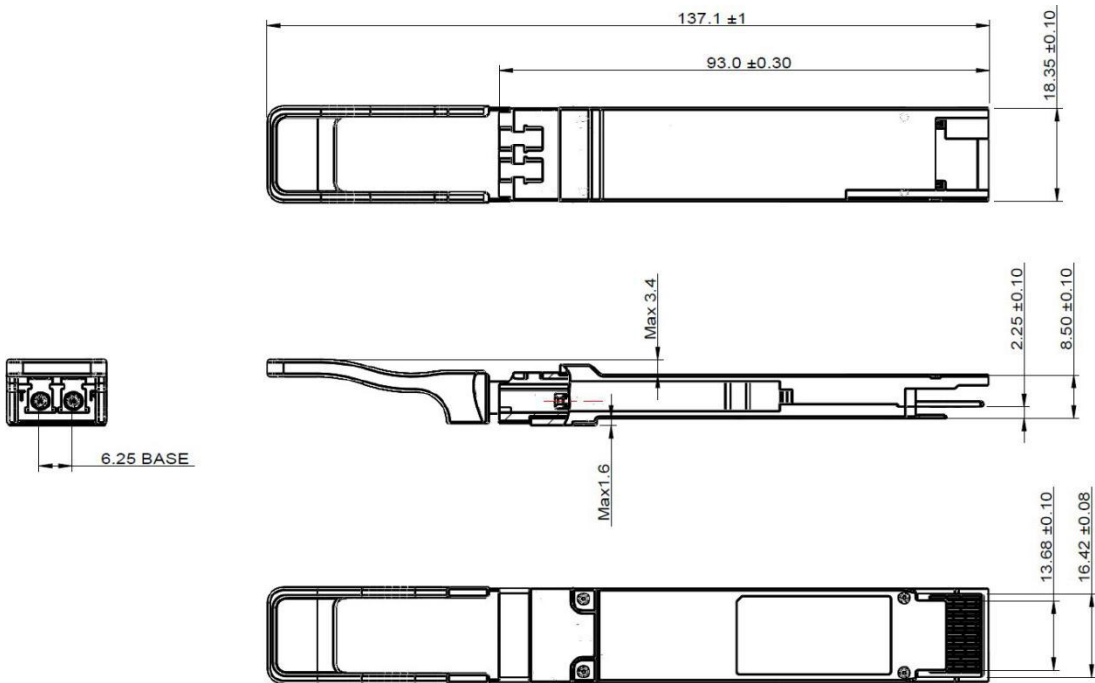## IX. Diagram Mechanical Dimensions

Figure 5. Mechanical Outline

X. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

XI. Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Test Center

FS.COM transceivers are tested to ensure connectivity and compatibility in our test center before shipped out. FS.COM test center is supported by a variety of mainstream original brand switches and groups of professional staff, helping our customers make the most efficient use of our products in their systems, network designs and deployments.
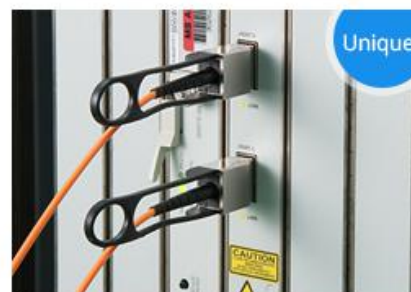
The original switches could be found nowhere but at FS.COM test center, eg: Juniper MX960 & EX 4300 series, Cisco Nexus 9396PX & Cisco ASR 9000 Series, HP 5900 Series & HP 5406R ZL2 V3(J9996A), Arista 7050S-64, Brocade ICX7750-26Q & ICX6610-48, Avaya VSP 7000 MDA 2, etc.

Cisco ASR 9000 Series(A9K-MPA-1X40GE)

ARISTA 7050S-64(DCS-7050S-64)

Juniper MX960

Brocade ICX 7750-26Q

Extreme Networks X670V VIM-40G4X

Mellanox M3601Q

Dell N4032F

HP 5406R ZL2 V3(J9996A)

AVAYA 7024XLS(7002QQ-MDA)

Test Assured Program

FS.COM truly understands the value of compatibility and interoperability to each optics. Every module FS.COM provides must run through programming and an extensive series of platform diagnostic tests to prove its performance and compatibility. In our test center, we care of every detail from staff to facilities—professionally trained staff, advanced test facilities and comprehensive original-brand switches, to ensure our customers to receive the optics with superior quality.

Our smart data system allows effective product management and quality control according to the unique serial number, properly tracing the order, shipment and every part.
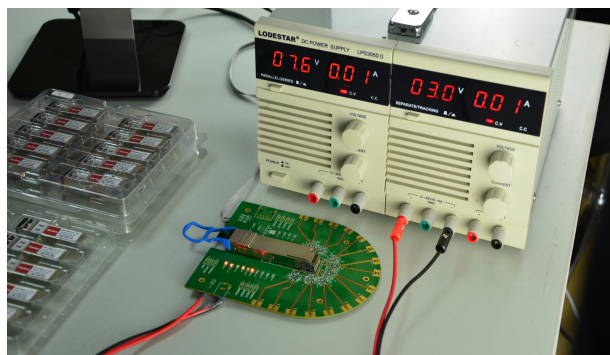
Our in-house coding facility programs all of our parts to standard OEM specs for compatibility on all major vendors and systems such as Cisco, Juniper, Brocade, HP, Dell, Arista and so on.
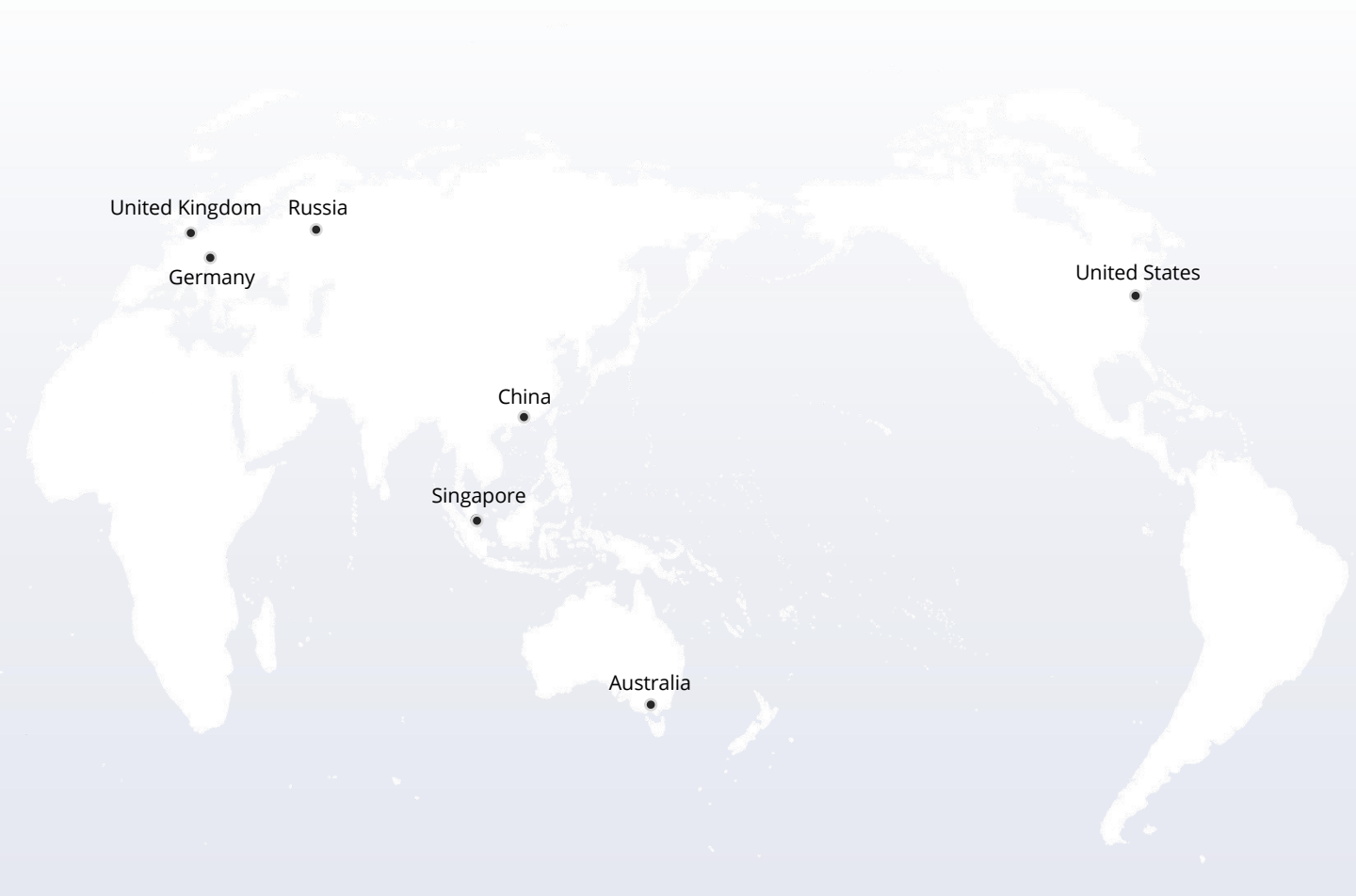

With a comprehensive line of original-brand switches, we can recreate an environment and test each optics in practical application to ensure quality and distance.

The last test assured step to ensure our products to be shipped with perfect package.

FS

Order Information

Part Number	Description
QSFPDD-SR8-400G	QSFP-DD 400GBASE-SR8 850nm 100m Transceiver
QSFPDD-DR4-400G	QSFP-DD 400GBASE-DR4 1310nm 500m Transceiver
QSFPDD-XDR4-400G	QSFP-DD 400GBASE-DR4+ 1310nm 2km Transceiver
QSFPDD-FR4-400G	QSFP-DD 400GBASE-FR4 1310nm 2km Transceiver
QSFPDD-LR4-400G	QSFP-DD 400GBASE-LR4 1310nm 10km Transceiver
QSFPDD-LR8-400G	QSFP-DD 400GBASE-LR8 1310nm 10km Transceiver

United Kingdom   Russia

          Germany   United States

                                        China

                              Singapore

                                        Australia

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