

400G QSFP-DD to QSFP-DD Active Optical Cable (AOC)



Application

- Data Centers and Cloud Networks
- Other 400G Interconnect Requirement

Features

- Up to 53.125Gbps Data Rate per Channel by PAM4 Modulation
- Support 400GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PD Array
- DDM Function Implemented
- Hot-pluggable QSFP-DD Form Factor
- Maximum Link Length of 100m OM4 (MMF) Fiber
- Low Power Dissipation: <11W
- Single +3.3V Power Supply
- Operating Temperature Range: 0°C~+70 °C
- Compliant with ROHS10

Description

400G QSFP-DD to 400G QSFP-DD Active Optical Cable enables low-power, high-reliability and high-speed interconnections over very thin copper cables without using any optical components. It is designed for relatively short connection, offering high-density solution alternative for system providers and customers implementing 400G in datacenters and Cloud Networks. It is compliant with IEEE 802.3cd, OIF-CEI-04.0, QSFP-DD MSA and QSFP-DD-CMIS-rev4p0.

Products Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Unit	Min.	Max.
Storage Temperature Rang	Ts	°C	-20	+85
Relative Humidity	RH	%	0	85
Power Supply Voltage	V _{CC}	V	-0.5	+4.0

II. Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
Operating Case Temperature Range	Tca	°C	0	/	70
Power Supply Voltage	V _{CC}	V	3.135	3.3	3.465
Bit Rate (Per Channel)	BR	GBd	26.5625		
Humidity	Rh	%	5		85
Fiber Bend Radius	Rb	cm	3		

III. Electrical Specifications

Parameter	Symbol	Units	Min.	Typ.	Max.	Notes
Supply Voltage	V _{CC} V _{CC3.3-Tx} V _{CC3.3-Rx}	V	3.135	3.3	3.465	
Power Consumption	Pc	W		9.5		Per-end

Parameter	Symbol	Units	Min.	Typ.	Max.	Notes
Transceiver Power-on Initialize Time		ms			2000	
Transmitter						
Differential Peak-to-peak Input Voltage Tolerance		mV	900			
Differential Termination Mismatch					10%	
Differential Input Return Loss(SDD11)		dB				See CEI-56G-VSR
Common-mode to Differential Conversion and Differential to Common-mode Conversion(SCD11, SDC11)		dB				See CEI-56G-VSR
Receiver						
Differential Peak-to-peak Output Voltage		mV			900	
DC Common Mode Voltage	V _{cm}	mV	-350		2850	
AC Common Mode Noise, RMS		mV			17.5	
Differential Termination Mismatch		%			10	
Differential Output Return Loss (SDD22)		dB				See CEI-56G-VSR
Common-mode to Differential Conversion and Differential to Common-mode Conversion(SCD22, SDC22)		dB				See CEI-56G-VSR
IIC Communication						
IIC Clock Frequency		KHZ		400	1000	
Clock Stretching		us			500	
Data Hold Time		ns				

IV. Principle Diagram

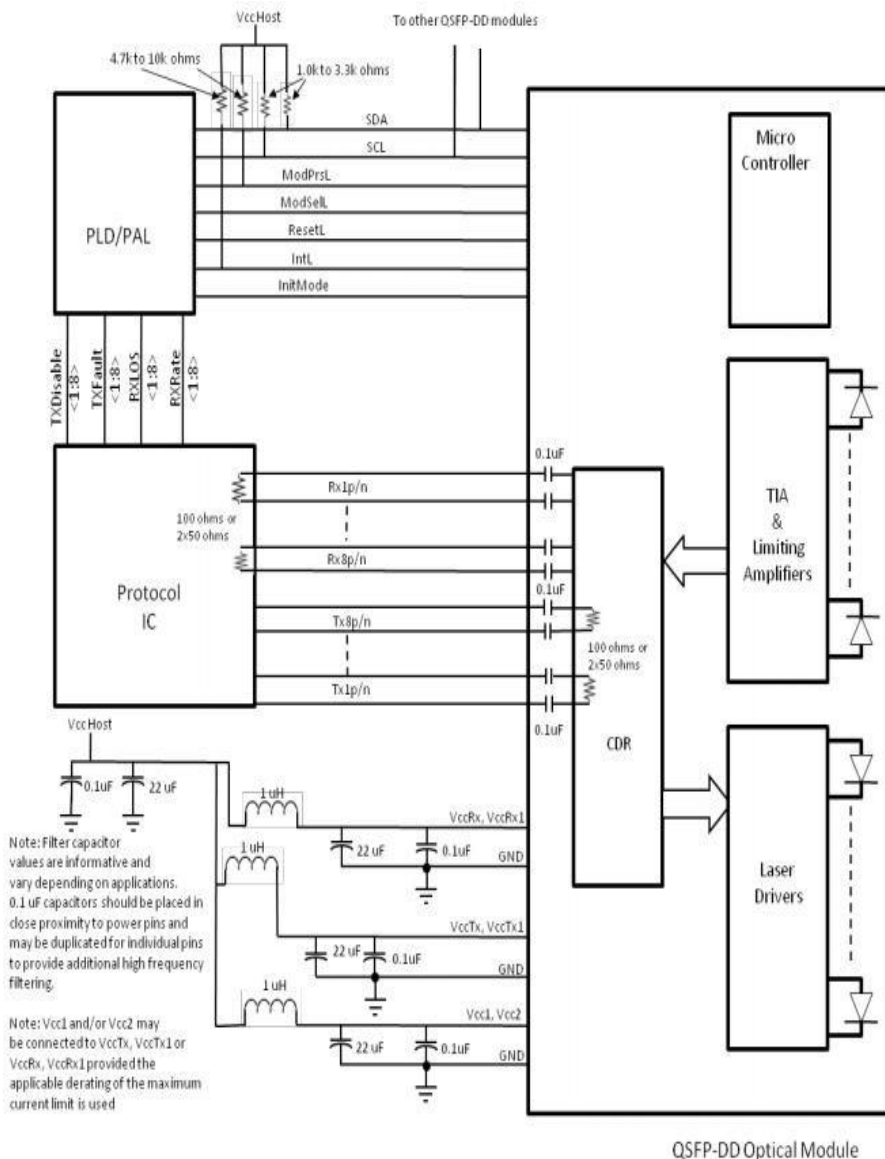


Figure 1. Module Principle Diagram

V. Pin Description

Pin	Logic	Symbol	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTTL-I	ModSelL	Module Select	
9	LVTTTL-I	ResetL	Module Reset	
10		V _{cc} Rx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-wire Serial Interface Data	
13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-0	GND	Ground	
18	CML-0	Rx1p	Receiver Non-Inverted Data Output	

Pin	Logic	Symbol	Description	Note
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0LVTTTL-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	
27	LVTTTL-0	ModPrsL	Module Present	
28	LVTTTL-0	IntL	Interrupt	
29		V _{CC} Tx	+3.3 V Power Supply Transmitter	2
30		V _{CC} 1	+3.3 V Power Supply	2
31	LVTTTL-I	InitMode	Initialization Mode; In Legacy QSFP Applications, the IntiMode Pad is Called LPMode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	

Pin	Logic	Symbol	Description	Note
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data output	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Dataoutput	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		V _{CC} Rxx1	+3.3V Power Supply Receiver	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	
53	CML-0	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1

Pin	Logic	Symbol	Description	Note
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	
56	CML-0	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-0	Rx6n	Receiver Inverted Data Output	
60	CML-0	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-0	Rx8n	Receiver Inverted Data Output	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For future use	3
67		VccTx 1	+3.3 V Power Supply Transmitter	2
68		Vcc2	+3.3 V Power Supply	2
69		Reserved	For Future Use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Inverted Data Input	
72	CML-I	Tx7n	Transmitter Non-Inverted Data Output	

Pin	Logic	Symbol	Description	Note
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Inverted Data Input	
75	CML-I	Tx5n	Transmitter Non-Inverted Data Output	
76		GND	Ground	1

Notes

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connected these directly to the host board signal common ground plane.
2. VCCR_x, VCCR_{x1}, VCC1, VCC2, VCCT_x, and VCCT_{x1} shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VCCR_x, VCCR_{x1}, VCC1, VCC2, VCCT_x, and VCCT_{x1} may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.

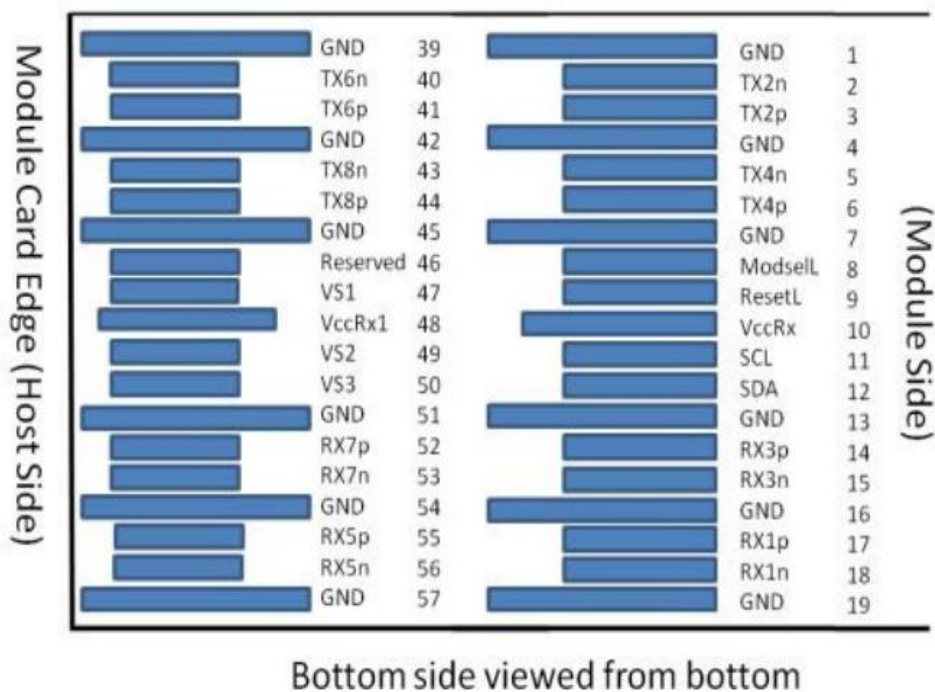
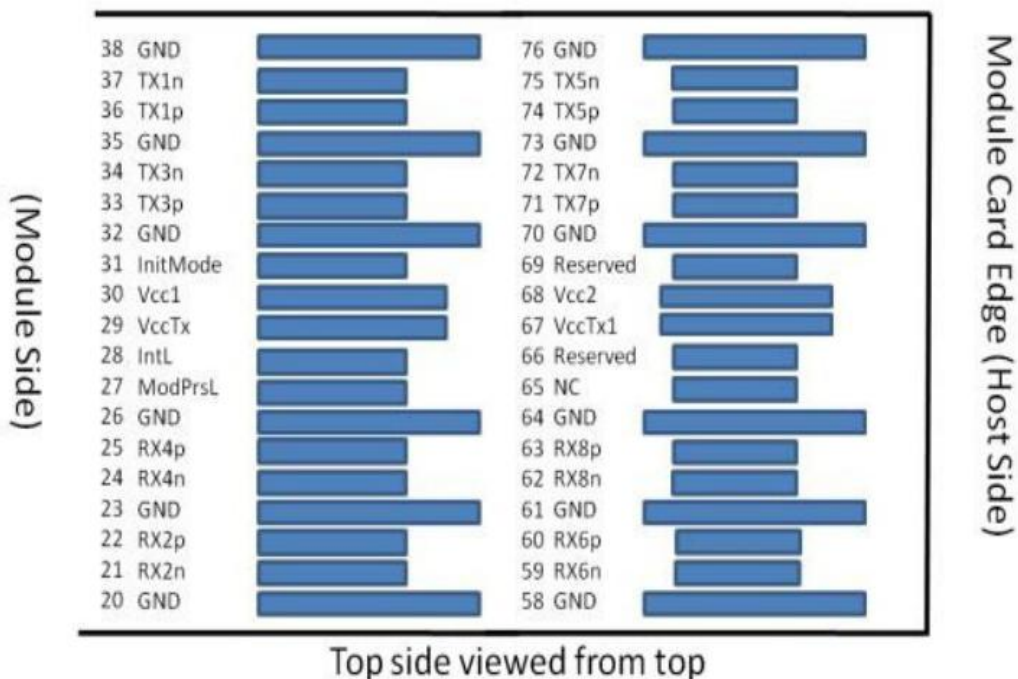


Figure 2. Electrical Pin-out Details

VI. Module Memory Map

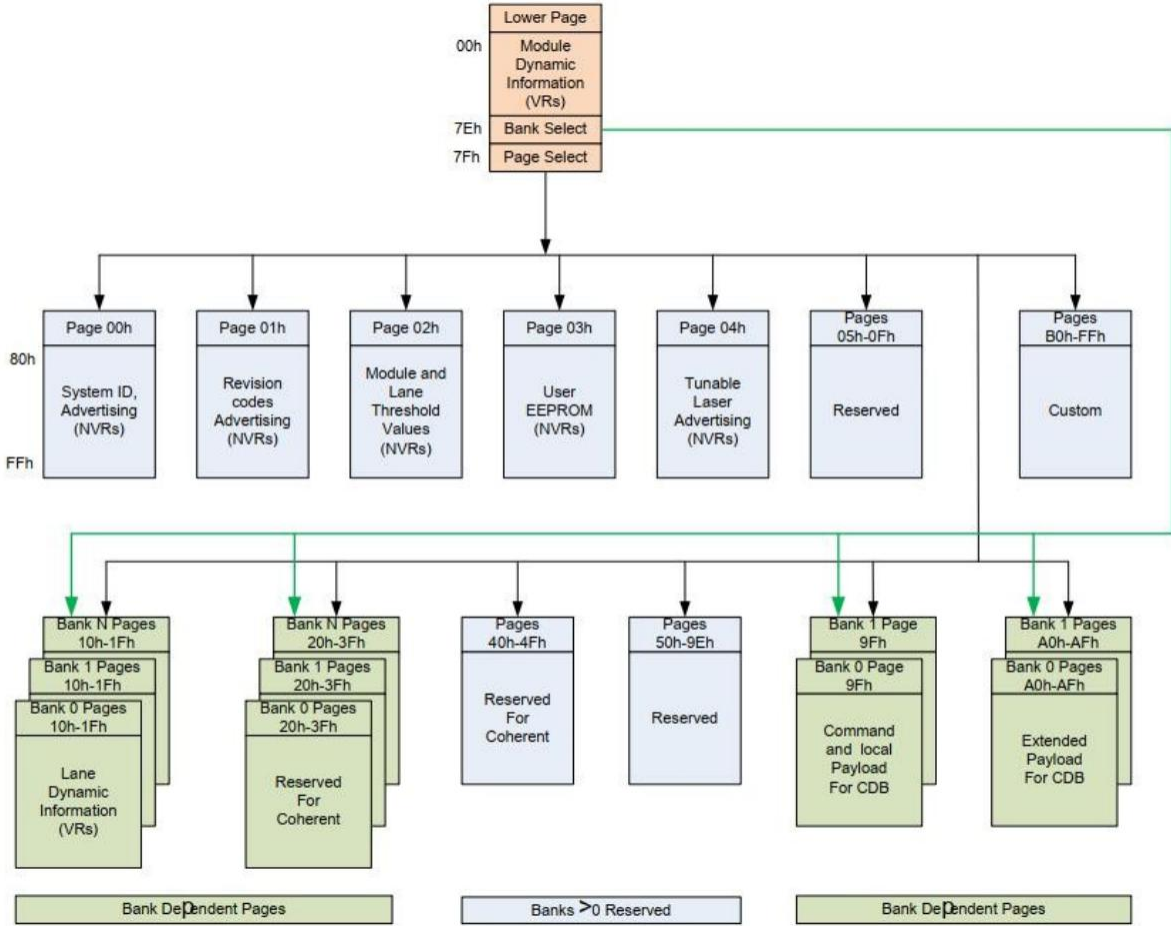


Figure 3. Digital Diagnostic Memory Maps

VII. Host Board Power Supply Filtering

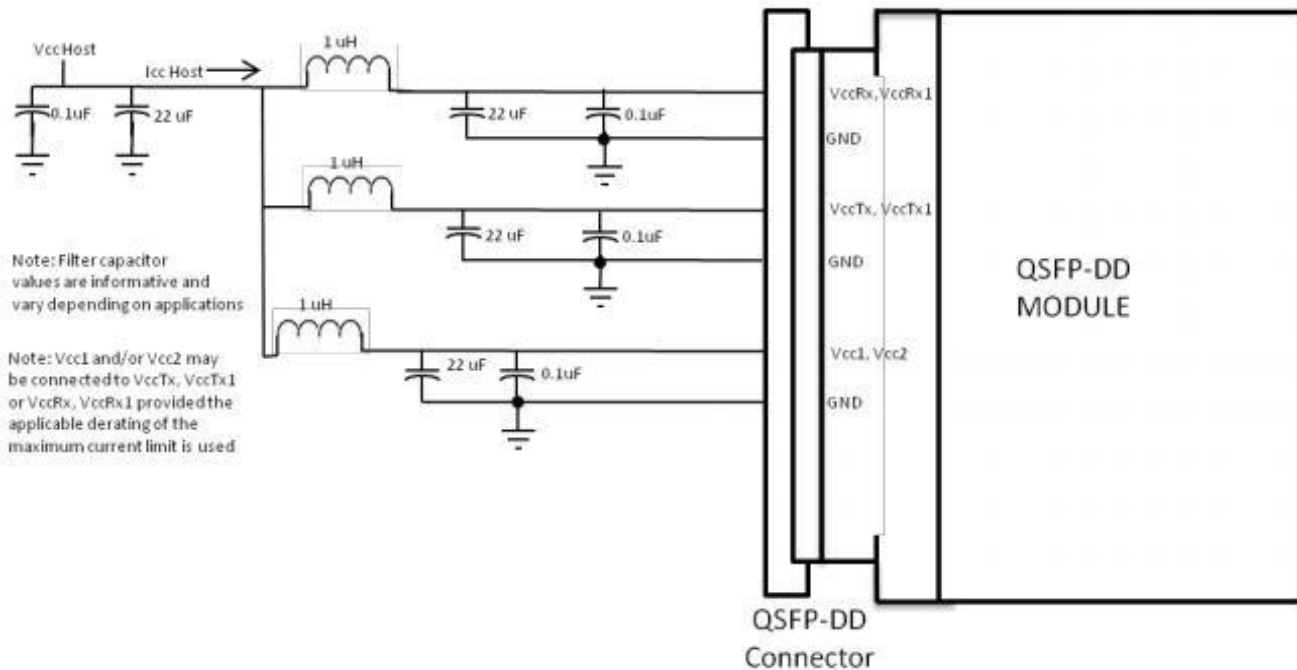
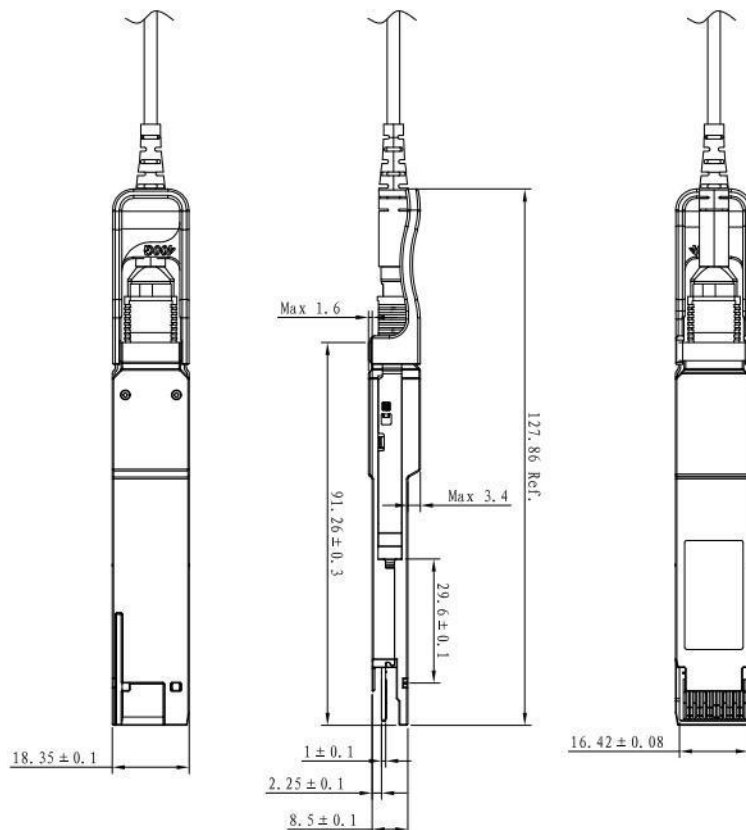


Figure 4. Digital Diagnostic Memory Map

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

VIII. Mechanical Cable Characteristics



Unit: mm

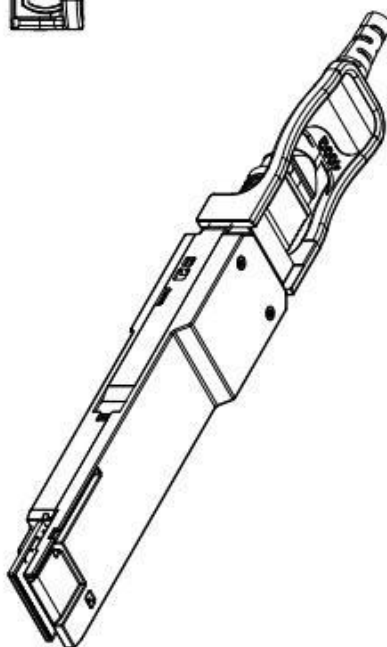


Figure 5. Package Outline

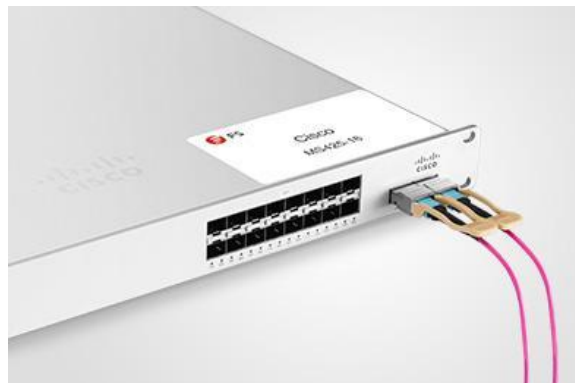
Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.



Cisco Catalyst C9500-24Y4C



Cisco MS425-16



Brocade VDX 6940-144S



Dell EMC Networking Z9100-ON



Force@tm S60-44T

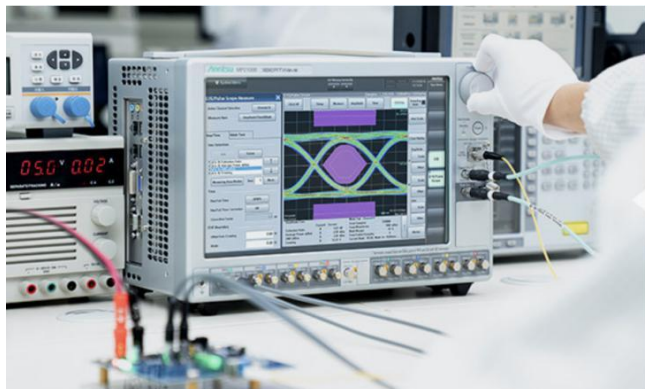


HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the [Test Bed](#) PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Signal Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator to ensure the input and output signal quality.

- Eye Pattern Measurements: jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic changes in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0 °C to 70 °C
- Extended: -5 °C to 85 °C
- Industrial: -40 °C to 85 °C



3. Transfer Rate and Protocol Testing

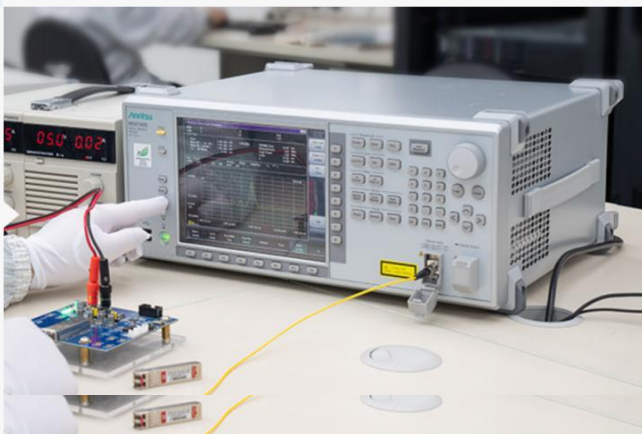
Test the actual transfer data rate and the transmission ability under different protocols with Network Master Pro.

- Ethernet
- Fibre Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

Part Number	Data Rate	Length	Connector Type	Temp. Range	Cable Jacket
QSFP-DD-AO01	Up to 400G	1m	Active Copper	0-70°C	LSZH
QSFP-DD-AO03	Up to 400G	3m	Active Copper	0-70°C	LSZH
QSFP-DD-AO05	Up to 400G	5m	Active Copper	0-70°C	LSZH
QSFP-DD-AO10	Up to 400G	10m	Active Copper	0-70°C	LSZH
QSFP-DD-AO15	Up to 400G	15m	Active Copper	0-70°C	LSZH
QSFP-DD-AO20	Up to 400G	20m	Active Copper	0-70°C	LSZH
QSFP-DD-AO30	Up to 400G	30m	Active Copper	0-70°C	LSZH
QSFP-DD-AO50	Up to 400G	50m	Active Copper	0-70°C	LSZH
QSFP-DD-AO70	Up to 400G	70m	Active Copper	0-70°C	LSZH
QSFP-DD-AO100	Up to 400G	100m	Active Copper	0-70°C	LSZH



 <https://www.fs.com>



The information in this document is subject to change without notice. FS has made all efforts to ensure the accuracy of the information, but all information in this document does not constitute any kind of warranty.