

400G QSFP-DD Passive Loopback Testing Module

QSFP-DD-LB



Application

- Board and System Level Testing
- Test and Measurement
- Acc. to QSFP-DD MSA
- Connecting / Short circuit Testing
- Signal Integrity requirements for single Loopback acc. to IEEE 802.3 bj and IEEE 802.3 cd

Features

- DC Test interval: 100%
- Testing Voltage: 25VDC
- Time: 500µsec
- Lower threshold: 100Ω Upper threshold: 20kΩ

Capacitor parameter:

- Time factor: 300µsec
- Voltage: 3V
- Programmable power consumption: 1.5W-15W / Thermal shutdown is set to 85° C
- Dual LED indicator: power mode (color) / module deselect (blinking).
- Other options on request diagnostic functions (IO extender over I²C bus)
- Guaranteed mating cycles: 200
- Temperature: 0-85° C

Signals

I. Status LED

Colour / State	Meaning
Green (Solid)	Module is operating in low power mode , no Alarm Flag set €Regarding to MSA
Red (Solid)	Module is operating in high power mode , no Alarm Flag set €Regarding to MSA
Green/Red (Blinking)	Signifies that an Alarm Flag is set.

II. Low Speed Signals

Befehl	Parameter	Bedeutung
Pin Number QSFP Connector	Signal Name	Description
8	ModSelL*	Host can select the LB Module through this Pin. ModSelL = low € LB selected ModSelL = high € LB deselected
9	ResetL	Resets the LB module by pulling the signal low. ResetL is pulled to VCC in the LB Module.
11,12	SDA,SCL	I2C Bus to communicate with the PCA9654E and the microcontroller.
27	ModPrsL	Signal is pulled to GND in the LB module and pulled high in the Host module.
28	IntL	Indicates a possible module operation fault when pulled low by the LB module. Pulled high in the host board.
31	LPMoDe/InitMoDe*	Pulled high in the LB module. High state indicates that module is in low power mode. When pulled low by the Host LB module enters high power mode.

Note:
 The State of InitMode and ModSelL does not affect any operation in the module.
 ModSelL has no function to deselect the module by HW Pin. The Pin status is just reported in the digital state register.

III. Monitored Values in Loopback Module

Page	Address @ LowMemory Map	Description
Lower MemoryMap	12-13	Internally monitored module temperature MSB @ low address
Lower MemoryMap	14-15	Internally monitored module temperature 2 MSB @ low address
Lower Memory Map	16-17	VCCR _X * € internally measured Voltage MSB @ low address
Lower Memory Map	18-19	VCCT _X * € internally measured Voltage MSB @ low address
Lower Memory Map	22-23	VCC € internally measured Voltage MSB @ low address

Note: Not implemented with current hardware.

IV. Software Reset

Page	Address @ LowMemory Map	Description
Lower MemoryMap	26	Set Bit 3 through the host to cause the soft reset

V. Power Class Selection Function.

Page	Byte	Bits	Description	Meaning
Upper Page 0	200	7-5	Module Card Power Class	000: Power class 1 (1.5 W maximum) 001: Power class 2 (3.5 W maximum) 010: Power class 3 (5.0 W maximum) 011: Power class 4 (7.0 W maximum) 100: Power class 5 (10.0 W maximum) 101: Power class 6 (12.0 W maximum) 110: Power class 7 (14.0 W maximum) 111: Power class 8 (16.0 W maximum)

VI. Alarm Indicators

Page	Address @ LowMemory Map	Description
Lower Memory Page	7	Temperature Alarm/Warning masking bits Bit 7 € VCC High Alarm Bit 6 € VCC Low Alarm Bit 3 € Temp High Alarm* Bit 2 € Temp Low Alarm

Note: The thermal shutdown is set to 85° C. This may cause thermal damage to the Hardware used in.

VII. Digital State / Transection Register

Page	Address	Bits	Description	Type
Upper Page 0xFF	225	5	ModSelL transection Read 0b: No Edge detect Read 1b: Either rising or falling edge detect Write 0b: No effect Write 1b: Clear the register	RW
		4	InitMode transection Read 0b: No Edge detect Read 1b: Either rising or falling edge detect Write 0b: No effect Write 1b: Clear the register	RW
		3	ResetL transection Read 0b: No Edge detect Read 1b: Either rising or falling edge detect Write 0b: No effect Write 1b: Clear the register	RW
		2	ModSelL pin status 0b: logical 0 1b: logical 1	RO
		1	InitMode pin status 0b: logical 0 1b: logical 1	RO
		0	ResetL pin status 0b: logical 0 1b: logical 1	RO

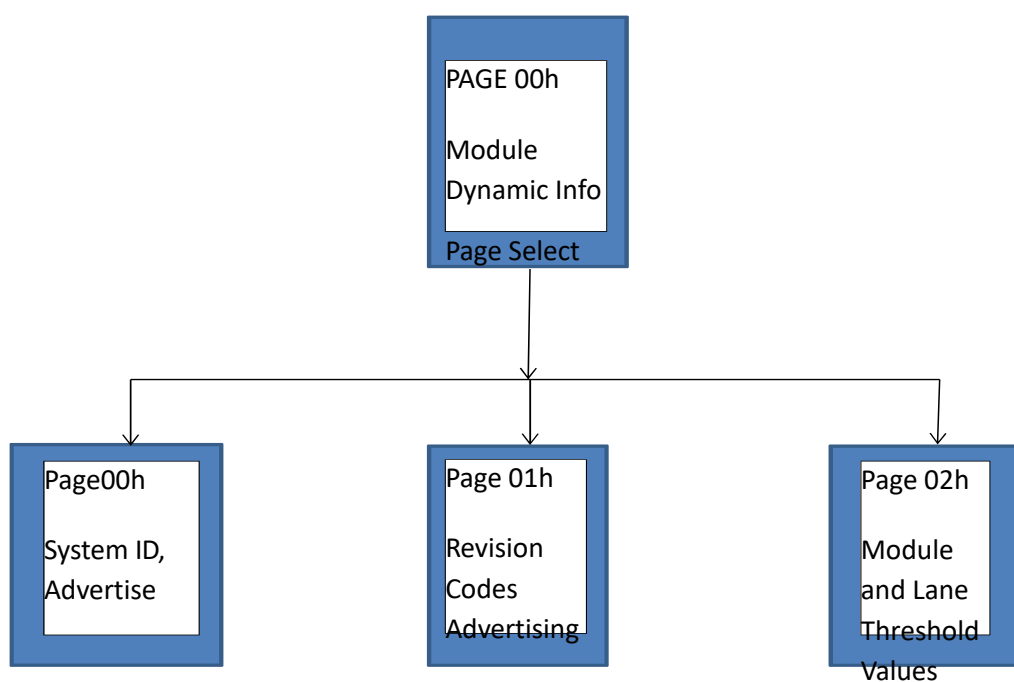
VIII. Digital Control Register

Page	Address	Bits	Description	Type
Upper Page 0xFF	254	7-6	ModPrsL control 0xb: Normal operation 10b: Force the ModPrsL to logic 0 11b: Force the ModPrsL to logic 1	RW
		5-4	IntL control 0xb: Normal operation 10b: Force the IntL to logic 0 11b: Force the IntL to logic 1	RW

IX. Guaranteed maximum insertion

Page	Address	Description
Upper Page 0xFF	252	Guaranteed maximum insertion inhex MSB
	253	Guaranteed maximum insertion inhex LSB

Memory Map



I.Lower Memory Map

Byte	Name of field	Value	Description
0	Identifier	0x18	QSFP-DD
1	Version ID	0x30	
2	Status / Info Byte	0x04	Paged Memory, INTL notsupported
3	Interrupt Flag		0b: No Interrupt1b: Interrupt
3-6	No Flags	0x00	
7	Interrupt Flag VCC & Temp	0xXX	
8	Interrupt Flag Not implemented	0x00	
9	Interrupt Flag Not implemented	0x00	
10-11	Reserved	0x00	
12-13	Module Monitor Temperature 1	0xFFFF	16-bit signed twos complement value in increments of 1/256.from -128C to +128C
14-15	Module Monitor Temperature 2	0xFFFF	16-bit signed twos complement value in increments of 1/256.from -128C to +128C
16-17	Voltage Monitor VCCR _X	0xFFFF	Full 16 bit value (0 – 65535) with LSB equal to 100uVolt, yielding a total measurement range of 0 to+6.55 Volts.
18-19	Voltage Monitor 2 VCCT _X	0xFFFF	
20-21	Module Monitor not supported	0x0000	
22-23	Module Monitor 3 VCC	0xFFFF	
24	Not implemented	0x00	
25	Not implemented	0x00	
26	Software Reset	0x00	
27-30	Module Global Controls	0xXX,0xXX	

31-52	Module Flag Masks	0x00	
53	Reserved	0x00	
54	Custom	0x00	
55-63	Reserved	0x00	
64-84	Custom	0x00	
85	Module Advertising code	0x03	
86	Host electrical Interface	0x1D	
87	Module Media Interface	0x01	
88	Host/Media Lane Count	0x88	
89	Lane assignment	0xFF	Not supported
90	Host Electrical Interface Code	0x1D	
91	Module Media Interface Code	0x01	
92	Host/Media Lane count	0x88	
93	Lane assignment	0xFF	
94	Host Electrical Interface	0x00	
95	Module Media Interface	0x00	
96	Host/Media Lane Count	0x00	
97	Reserved		
98	Host Electrical Interface	0x00	
99	Module Media Interface	0x00	
100	Host/Media Lane Count	0x00	

101	Reserved	0x00	
102	Host Electrical Interface Code	0x00	
103	Module Media Interface	0x00	
104	Host/Media Lane Count	0x00	
105	Reserved	0x00	
106	Host Electrical Interface	0x00	
107	Module Media Interface Code	0x00	
108	Host/Media Lane Count	0x00	
109	Reserved	0x00	
110	Host Electrical Interface Count	0x00	
111	Module Media Interface	0x00	
112	Host/Media Lane Count	0x00	
113	Reserved	0x00	
114	Host Electrical Interface Count	0x00	
115	Module Media Interface	0x00	
116	Host/Media Lane Count	0x00	
117	Reserved	0x00	
118-126	Not implemented	0x00	
127	Page select	0xFF	

II. Upper Memory Page 0

Byte	Description	Value	Comment
128	Identifier	0x18	QSFP-DD
129-144	Vendor Name	ASCII String	
145-147	Vendor OUI	IEEE Code	ASCII
148-163	Vendor PN	Part NumberVendor	ASCII
164-165	Vendor rev	Vendor serialNumber	
166-181	Vendor Serial Number	ASCII String	ASCII
182-187	Date Code	ASCII STRING	ASCII
188-189	Lot Code	ASCII	ASCII
190-199	CLEI CODE		Not implemented
200	Power Set Bit	0bxxx00000	
201	MAX Power Byte 16.0 Win 0.1W steps	0xA0	16 W
202	Cable Assembly length	0x00	
203	Connector type	0x23	
204	ATTN. at 5 GHz signal rate	0x00	0 dB
205	ATTN. at 7 GHz	0x00	0 dB
206	ATTN. at 12.9 GHz	0x00	0 dB
207	ATTN. at 25.8 GHz	0x00	0 dB
208	Cable ATTN.	0x00	0 dB
209	Reserved	0x00	

210	Near End Implementation	0x00	
211	Far End implementation	0x00	
212	Technology Copper Cableunequalized		
213-220	Not Implemented	0x00	
221	Custom	0x00	
222	CRC	0xxx	Byte 128-221
223-255	Custom	0x00	

III.Upper Memory Page 1

Byte	Description	Value
128	Software Major Revision	0x01
129	Software Minor Revision	0x00
130	Hardware Major revision	0x01
131	Hardware Minor revision	0x00
132-140	Not implemented	
141	Implemented memory pages	0x03
142-145	Not implemented	0x00
146	Maximum Module temperature	0x55
147	Maximum Module temperature	0x00
148-158	Not implemented	0x00
159	Implemented Monitors	0x00
160-255	Not implemented	0x00

IV. Upper Memory Page 2 (Threshold Values)

Byte	Description	Value
128-129	Temp Alarm High	MSB @ low address
130-131	Temp Alarm Low	MSB @ low address
144-145	VCC_RX High Alarm	MSB @ low address
146-147	VCC_RX LOW Alarm	MSB @ low address
160-161	VCC_TX High Alarm	MSB @ low address
162-163	VCC_TX Low Alarm	MSB @ low address
168-169	VCC_1 High Alarm	MSB @ low address
170-171	VCC_1 Low Alarm	MSB @ low address
172-254	Not Implemented	0x00
255	CRC	Byte 128-254

V. Upper Memory Page 3

Byte	Description	Value
128-255	Not implemented	

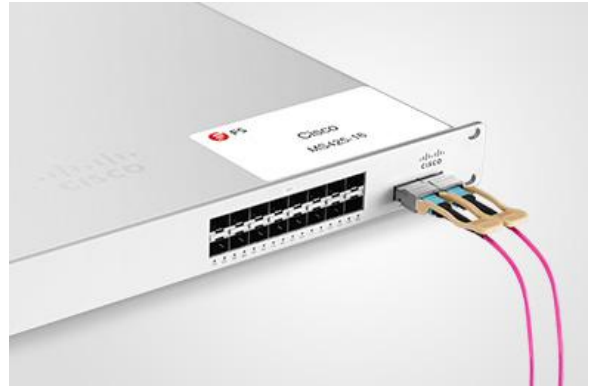
Test Center

I. Compatibility Testing

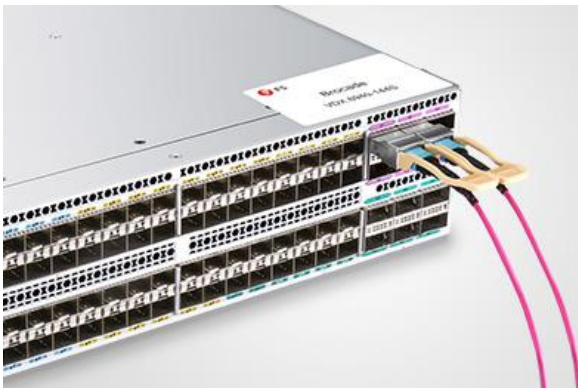
Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.



Cisco Catalyst C9500-24Y4C



Cisco MS425-16



Brocade VDX 6940-144S



Dell EMC Networking Z9100-ON



Force@tm S60-44T

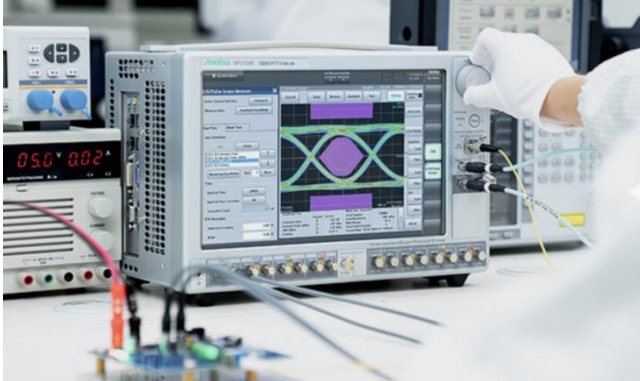


HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the [Test Bed PDF](#). It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Single Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator the input and output signal quality.

- Eye Pattern Measurements: Jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0°C to 70°C
- Extended: -5°C to 85°C
- Industrial: -40°C to 85°C



3. Transfer Rate and Protocol Testing

Test the actual transfer data rate and the transmission ability under different protocols with Networks Master Pro.

- Ethernet
- Fiber Channel
- SDH/SONET
- CPRI



4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

Part Number	Description
QSFP-DD-LB	QSFP-DD Loopback, 8x50 Gbps 1.5W - 15W, >0dB Attn



 <https://www.fs.com>



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