400GBase DR4 OSFP 1310nm 500m MTP/MPO-12 Transceiver

OSFP-DR4-400G-Si

Application

- 400G Ethernet
- Infiniband Interconnects
- Data Center and Enterprise Networking

Features

- Compliant with IEEE 802.3bs and OSFP MSA
- Four Parallel 1310nm Optical Lanes
- 8*53.125Gbps (PAM4) Electrical Interface (400GAUI-8), 4*106.25Gbps (PAM4) Optical Interface (1*12 APC MPO)
- Up to 500m Transmission on Single Mode Fiber (SMF) with FEC
- Maximum Power Consumption: 10W
- Operation Case Temperature: 0 to 70° C
- Compatible with CMIS 4.0 I2C Interface
- RoHS Compliant
- Laser Safety Class 1

Product Description

OSFP 400GBASE-DR4 silicon photonics transceiver is based on a new state-of-the-art silicon photonics (SiPh) platform. It uses SiPh chips that integrate a number of active and passive optoelectronic components. It is a cost-effective and lower power consumption solution for 400GBASE data center.

The 400GBASE-DR4 silicon photonics module supports link lengths of up to 500m SMF with MTP/MPO-12 connector. It is compliant with OSFP MSA, CMIS 4.0 I2C Interface and 400GAUI-8 standards. The 400 Gigabit Ethernet signal is carried over four parallel 1310nm optical lanes by one wavelength per lane. It can be used as 4x100G breakout to QSFP28-DR-100G.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Unit	Min.	Max.
Storage Temperature	℃	-40	85
Operating Relative Humidity	%	0	85
Power Supply Voltage	V	-0.5	3.63
Damage Threshold	dBm	5	

II. Recommended Operating Environment

Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	℃	0		70	
Power Supply Voltage	V	3.135	3.3	3.465	
Power Consumption	W			10	
Pre-FEC Bit Error Ratio			2.4E-4		
Post-FEC Bit Error Ratio			1E-12		1
Link Distance (DR4)	m	2		500	2

Notes

1. FEC is provided by host system.
2. FEC is required on host system to support maximum distance.

III. Electrical Characteristics

Parameter	Unit	Min.	Typical	Max.	Test point[1]	Notes
Transmitter						
Signaling Rate per Lane (Range)	GBd		26.5625 ±100 ppm		TP1	
Differential Pk-pk Input Voltage Tolerance	mVpp	900			TP1a	2
Differential Input Return Loss	dB		Equation (83E-5)		TP1	
Differential to Common Mode Input Return Loss	dB		Equation (83E-6)		TP1	
Differential Termination Mismatch	%			10	TP1	
Module Stressed Input Test			See120E.3.4.1		TP1a	3
Single-ended Voltage Tolerance Range	V	-0.4		3.3	TP1a	
DC Common Mode Voltage	mV	-350		2850	TP1	4
Receiver						
Signaling Rate per Lane (Range)	GBd		26.5625 ±100 ppm		TP4	
Peak-to-peak Differential Output Voltage	mVpp			900	TP4	
AC Common-Mode Output Voltage, RMS	mV			17.5	TP4	
Differential Output Return Loss			Equation(83E-2)		TP4	
Common to Differential Mode Conversion			Equation(83E-3)		TP4	
Differential Termination Mismatch	%			10	TP4	
Transition Time, 20% to 80%	ps	9.5			TP4	
Near-end ESMW (Eye Symmetry Mask Width)	UI		0.265		TP4	

Parameter	Unit	Min.	Typical	Max.	Test point[1]	Notes
Near-end Eye Height, Differential	mV	70			TP4	
Far-end ESMW (Eye Symmetry Mask Width)	UI		0.2		TP4	
Far-end Eye Height, Differential	mV	30			TP4	
Far-end Pre-cursor ISI Ratio	%	-4.5		2.5	TP4	
DC Common Mode Voltage	mV	-350		2850	TP4	4

Notes:

1. The location of TP1, TP1a and TP4 are defined in IEEE 802.3bs Figure 120E–5 and Figure 120E–6.
2. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets BER specified in IEEE 802.3bs 120E.1.1.
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

IV. Optical Characteristics

Parameter	Unit	Min.	Typical	Max.	Notes
Transmitter					
Signaling Rate, per Lane	GBd		53.125±100ppm		PAM4
TX Central Wavelength	nm	1304.5	1310	1317.5	
Side-mode Suppression Ratio (SMSR)	dB	30			
Average Launch Power, per Lane	dBm	-2.9		4	1
Outer Optical Modulation Amplitude (OMA_{Outer}), per Lane	dBm	-0.8		4.2	2
Launch Power in OMA_{Outer} Minus TDECQ, each Lane	dBm	-2.2			
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), per Lane	dB			3.4	3

Parameter	Unit	Min.	Typical	Max.	Notes
Average Launch Power of OFF Transmitter, per Lane	dBm			-15	
Extinction Ratio, per Lane	dB	3.5			
Optical Return Loss Tolerance	dB			21.4	
$RIN_{21.4}OMA$	dB/Hz			-136	
Transmitter Reflectance	dB			-26	
Receiver					
Signaling Rate, per Lane	GBd	53.125±100ppm			PAM4
RX Central Wavelength	nm	1304.5	1310	1317.5	
Damage Threshold	dBm	5			4
Average Receive Power per Lane	dBm	-5.9		4.0	5
Receiving Power (OMA_{Outer}) per Lane	dBm			4.2	
Receive Reflectance (max.)	dB			-26	
Receiver Sensitivity (OMA_{Outer}), per Lane (Max.)	dBm	Equation(1)			6
Stressed Receiver Sensitivity (OMA_{Outer}), per Lane	dBm			-1.9	7
Conditions of Stressed Receiver Sensitivity Test					
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test	dB		3.4		8
OMA_{Outer} of each Aggressor Lane	dBm			4.2	
LOS Assert	dBm	-15			

Parameter	Unit	Min.	Typical	Max.	Notes
LOS De-Assert	dBm			-8.9	
LOS Hysteresis	dB	0.5			

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or TDECQ < 1.1dB for an extinction ratio of < 5dB, the OMA_{Outer} (min) must exceed the minimum value specified here.

3. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

6. Receiver sensitivity (OMA_{Outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation (1), which is illustrated in Figure 1.

7. Measured with conformance test signal at TP3 for the BER equal to 2.4E-4.

8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

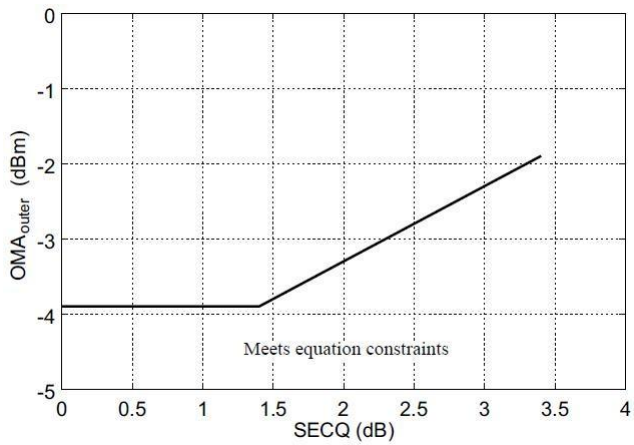


Figure 1. Illustration of Receiver Sensitivity Mask for 400G-DR4

= max(−3.9, − 5.3) (1) Where: RS is the receiver sensitivity, and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

V. Optical Interface

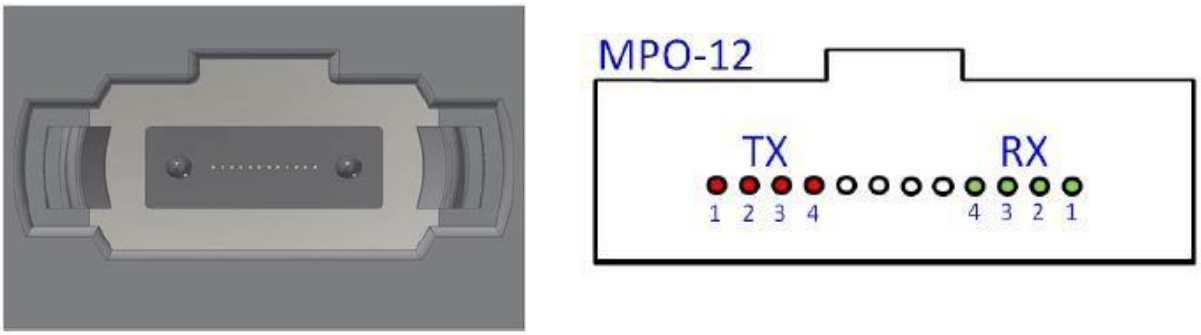


Figure 2: MPO-12 Single Row optical patch cord and module receptacle.

VI. Assignment and Description

The electrical interface of an OSFP module consists of a 60 contacts edge connector as illustrated by the diagram in Figure 3. It provides 16 contacts for 8 differential pairs of high-speed transmit signals, 16 contacts for 8 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 4 contacts for power and 20 contacts for ground.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.

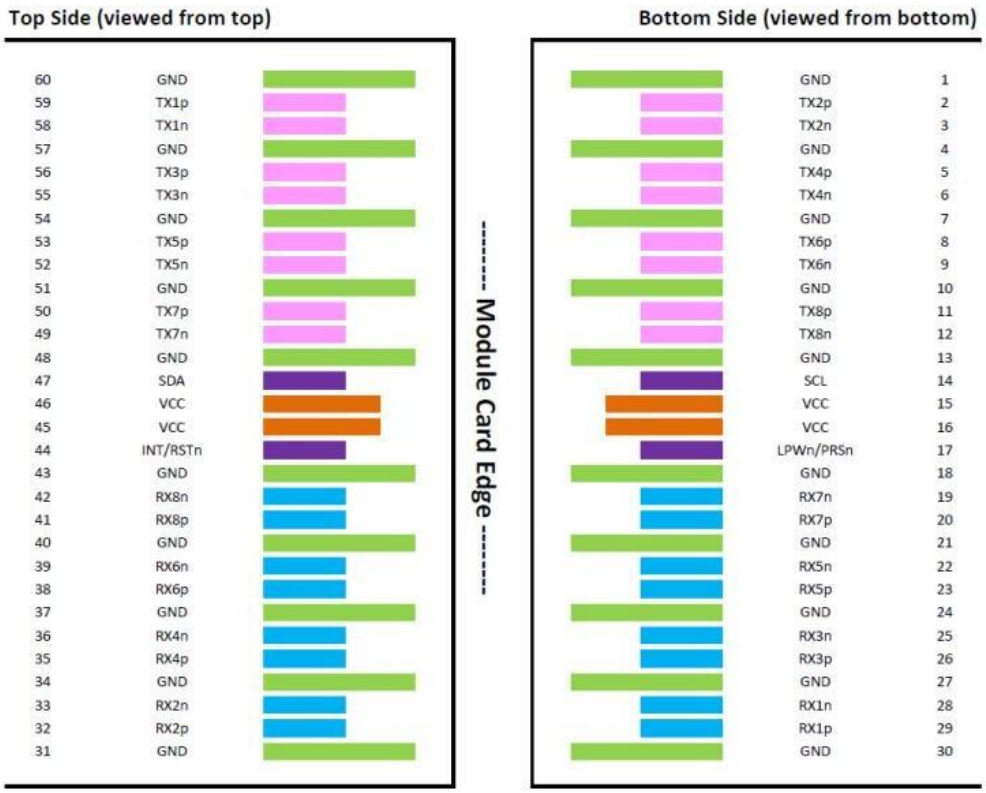


Figure 3： Module Pad Layout

VII. PIN Function Definitions

1. OSFP Module Signal Pin Descriptions

Name	Direction	Description
TX[8:1]p	Input	Transmit Differential Pairs From Host to Module.
TX[8:1]n	Input	
RX[8:1]p	Output	Received Ifferential Pairs From Module to Host.
RX[8:1]n	Output	
SCL	Bidir	2-wire Serial Clock Signal. Requires Pull-up Resistor to 3.3V on Host.
SDA	Bidir	2-wire Serial Data Signal. Requires Pull-up Resistor to 3.3V on Host.
LPWn/PRSn	Bidir	Multi-level Signal for Low Power Control From Host to Module and Module Presence Indication From Module to Host. This Signal Requires the Circuit as Described in Section 11.5.3
INT/RSTn	Bidir	Multi-level Signal for Interrupt Request From Module to Host and Reset Control From Host to Module. This Signal Requires the Circuit as Described in Section 11.5.2
V_{CC}	Power	3.3V Power for Module.
GND	Ground	Module Ground. Logic and Power Return Path.

2. OSFP Connector Pin List

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input From Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input From Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input From Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input From Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial Interface Clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with Pull-up Resistor on Host
15	VCC	3.3V Power		Power From Host	2	
16	VCC	3.3V Power		Power From Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	See Pin Description for Required Circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt/ Module Reset	Multi-Level	Bi-directional	3	See Pin Description for Required Circuit
45	VCC	3.3V Power		Power From Host	2	
46	VCC	3.3V Power		Power From Host	2	
47	SDA	2-wire Serial Interface Data	LVCMOS-I/O	Bi-directional	3	Open-Drain with Pull-up Resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input From Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input From Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input From Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter DataInverted	CML-I	Input From Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input From Host	3	
60	GND	Ground			1	

VIII. Recommended Power Supply Filter

Figure 4 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

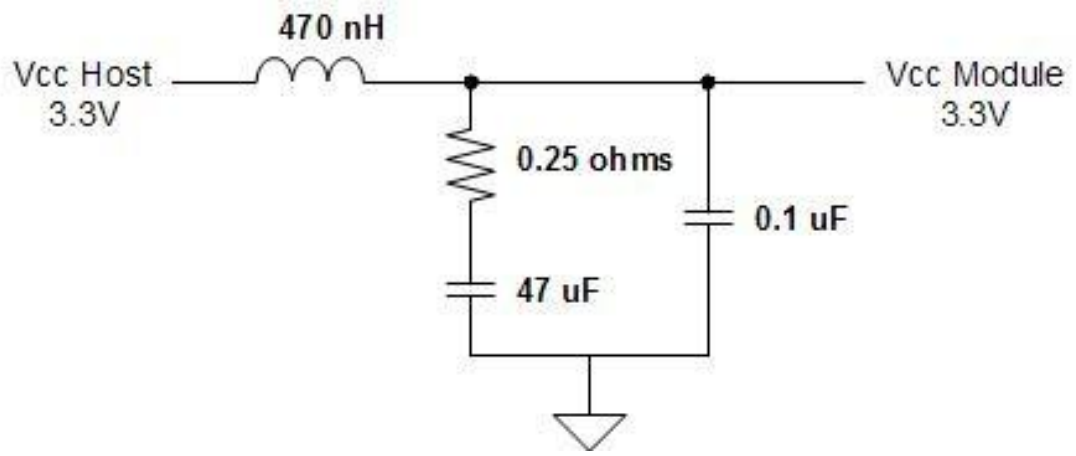
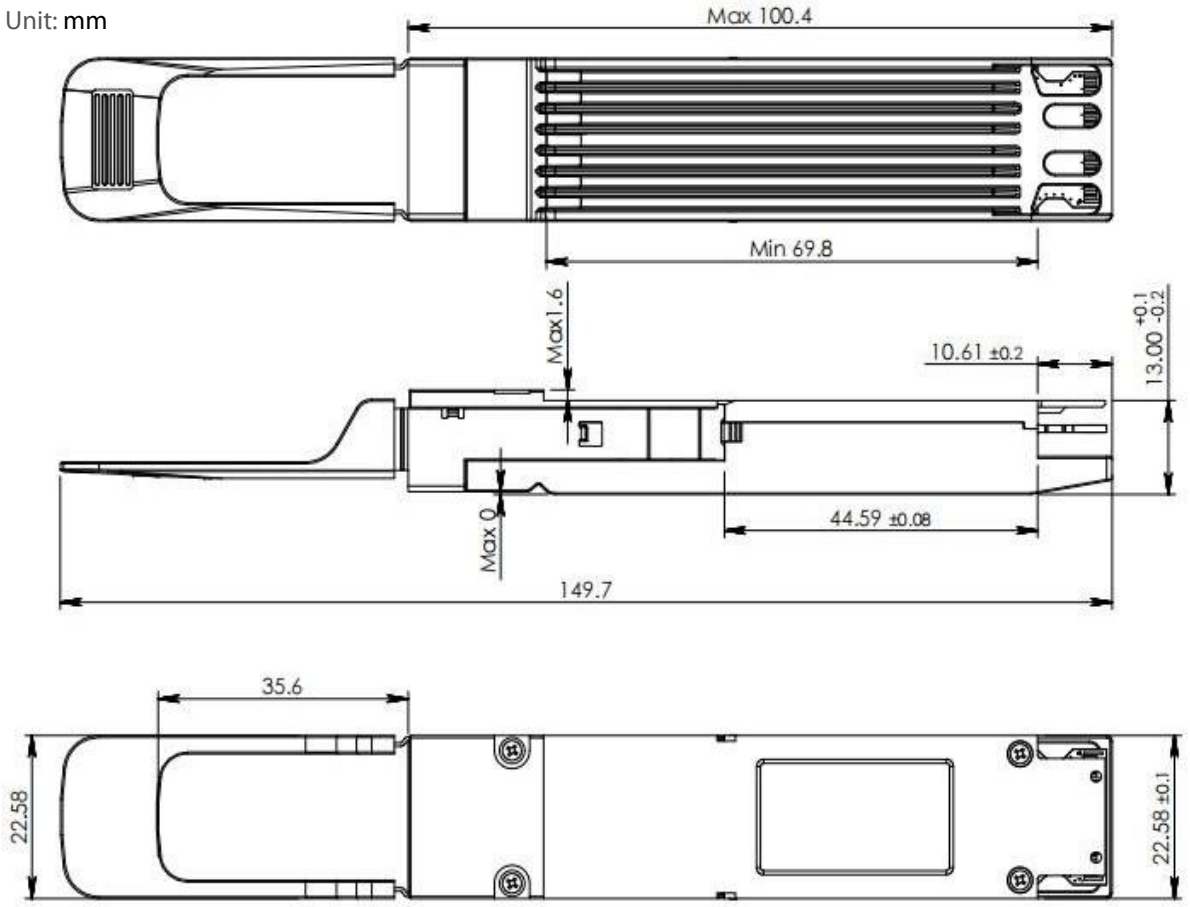


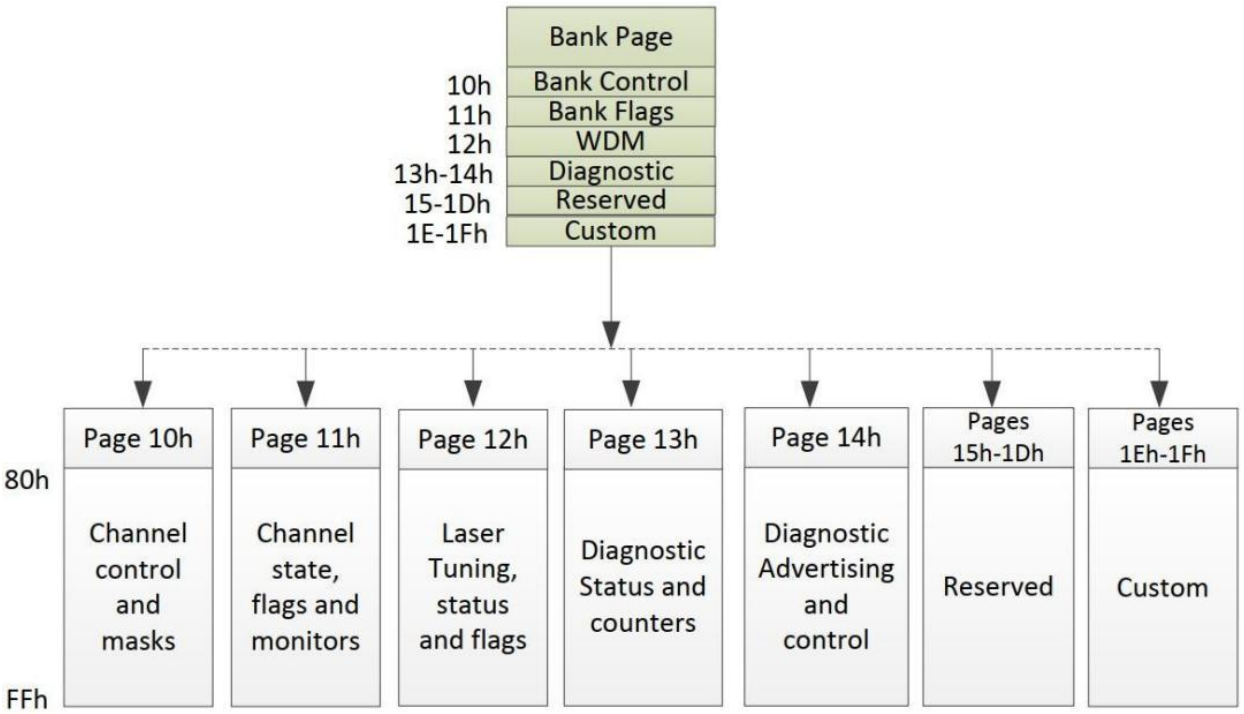
Figure 4: Host board power filter circuit

IX. Diagram Mechanical Drawing



X. Digital Diagnostic Functions

Parameter	Units	Error	Notes
Temperature Monitor	℃	±3	1LSB=1/256° C
Supply Voltage Monitor	V	±0.1	1LSB=100uV
Bias Current Monitor	mA	±10%	1LSB=2uA
TX Power Monitor	dBm	±3	1LSB=0.1uW
RX Power Monitor	dBm	±3	1LSB=0.1uW

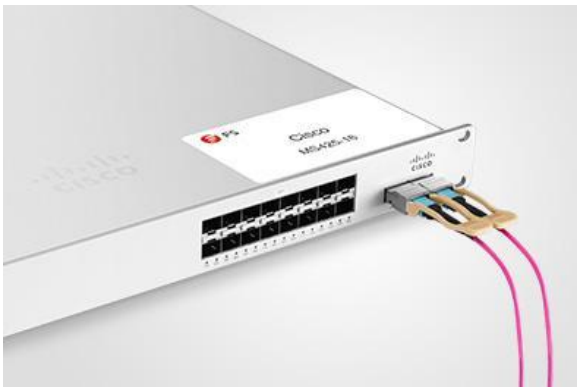


Test Center

I. Compatibility Testing

Each fiber optical transceiver has been tested in host device on site in FS Assured Program to ensure full compatibility with over 200 vendors.

Cisco Catalyst C9500-24Y4C



Cisco MS425-16

Brocade VDX 6940-144S

Dell EMC Networking Z9100-ON

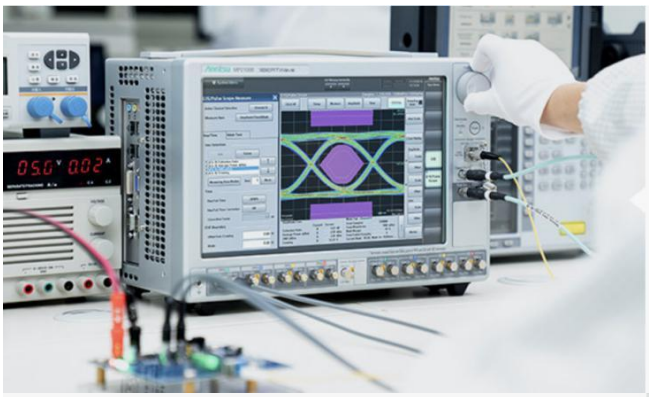
Force⑩tm S60-44T

HUAWEI S6720-30L-HI-24S

Above is part of our test bed network equipment. For more information, please click the Test Bed PDF. It will be updated in real time as we expand our portfolio.

II. Performance Testing

Each fiber optical transceiver has been fully tested in FS Assured Program equipped with world's most advanced analytical equipment to ensure that our transceivers work perfectly on your device.



1. TX/RX Signal Quality Testing

Equipped with the all-in-one tester integrated 4ch BERT & sampling oscilloscope, and variable optical attenuator to ensure the input and output signal quality.

- Eye Pattern Measurements: Jitter, Mask Margin, etc
- Average Output Power
- OMA
- Extinction Ratio
- Receiver Sensitivity
- BER Curve

2. Reliability and Stability Testing

Subject the transceivers to dramatic changes in temperature on the thermal shock chamber to ensure reliability and stability of the transceivers.

- Commercial: 0 °C to 70 °C
- Extended: -5 °C to 85 °C
- Industrial: -40 °C to 85 °C

3. Transfer Rate and Protocol Testing

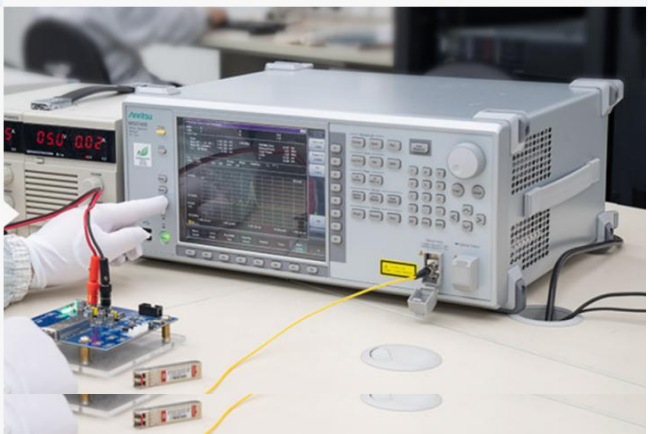
Test the actual transfer data rate and the transmission ability under different protocols with Network Master Pro.

- Ethernet
- Fibre Channel
- SDH/SONET
- CPRI

4. Optical Spectrum Evaluation

Evaluate various important parameters with the Optical Spectrum Analyzer to meet the industry standards.

- Center Wavelength, Level
- OSNR
- SMSR
- Spectrum Width



Order Information

Part Number	Description
QSFPDD-SR8-400G	QSFP-DD 400GBASE-SR8 850nm 100m Transceiver
OSFP400-DR4-Si	OSFP 400GBASE-DR4 1310nm 500m Silicon Photonics Transceiver
QDD-DR4-400G-Si	QSFP-DD 400GBASE-DR4 1310nm 500m Silicon Photonics Transceiver
QSFPDD-XDR4-400G	QSFP-DD 400GBASE-DR4+ 1310nm 2km Transceiver
QSFPDD-FR4-400G	QSFP-DD 400GBASE-FR4 1310nm 2km Transceiver
QSFPDD-LR4-400G	QSFP-DD 400GBASE-LR4 1310nm 10km Transceiver
QSFPDD-LR8-400G	QSFP-DD 400GBASE-LR8 1310nm 10km Transceiver
QSFPDD-ER8-400G	QSFP-DD 400GBASE-ER8 QSFP-DD PAM4 1310nm 40km Transceiver
QSFPDD-PLR4-400G	4x100GBASE-LR QSFPDD 1310nm 10km Transceiver

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